Jean-Loup Baer
January 2000

Personal
Born in France, September 12, 1936

Education
Diplome d'Ingénieur Electrotechnicien (Université de Grenoble) 1960
Diplome d'Ingénieur Mathématiques Appliquées (Université de Grenoble) 1961
License-es-sciences (Université de Grenoble) 1961
Doctorat 3^e Cycle (Université de Grenoble) 1963
Ph.D. (Major Engineering) (University of California at Los Angeles) 1968

Honors
U.C.L.A. Alumni Association Award for best Ph.D. in Engineering, 1969
Guggenheim Fellowship,1979-1980
IEEE Fellow 1992, ACM Fellow 1997

Employment at the University of Washington
Professor of Computer Science (1979-present); Boeing Pennell Professor (1995-present)
Chairman (1988-1993)
Associate Chairman (1978-79, 1980-81, 1982-84, 1985-87); Acting Chair (1981-82)
Adjunct Professor of Electrical Engineering (1983-present)
Associate Professor of Computer Science (1974-1979)
Director, Computer Science Teaching Laboratory (1974-1976)
Assistant Professor of Computer Science (1969-1974)

Representative Professional Activities
Editor-in-Chief, Journal of VLSI and Computer Systems 1982 - 1986, Editor, IEEE Trans. on Computers 1982 - 1986, Editor, IEEE Trans. on Parallel and Distributed Systems 1990 - 1994, Area editor, Journal of Parallel and Distributed Computing, 1987 - present, Associate Editor, Computer Languages 1975 - present
General Co-Chair, 1990 ISCA, Co-PC Chair 1983 ISCA, PC Chair HPCA-4 1998, Member of PC ISCA 1984, 1986, 1988, 1991, 1994; ASPLOS-III 1989, ICS 1991, 1994, IPPS 1995, 1996, HPCA 1996, SPAA 1999 etc.
Member of External Review Committee, University of Colorado, 1991, Oregon State University 1992, University of Minnesota 1992, 1998
Chair of ACM SIGARCH 1995-99; Member of ACM SGB-EC 1998-present
Member of Committee of Examiners for the GRE Board Computer Science Test 1994-present (Chair 1998 -present)

Student Supervision
20 Ph.D. completed, 20 M.S. completed. Ph.D. Graduates in the last 10 years:
S.-L. Min (1989), W.-H. Wang (1989), J. Bertoni (1991), R.Zucker (1992), T.-F. Chen (1993), C. Anderson (1995), X. Qin (1997), D.Lee (1999)

Recent Grants

- Boeing Computer Services "Resource Allocation in Shared-Memory Multiprocessors" $50,000 Mar 1988- Dec 1989
- NSF "Memory Management in Shared-Memory Multiprocessors" $190,985, July 1989-Dec 1991
- Apple Computer "Memory Management in Shared-Memory Multiprocessors" $45,000 (graduate fellowship) 1991-94
- NASA Research in Parallel Processing $20,000 (graduate fellowship) 1991
- N.S.F. "Memory Hierarchy in High-Performance Systems" $340,781 June 1991 - Dec 1994
- Intel Corp. "Reducing Memory through Prefetching" $75,000 June 1993 - June 1996
- N.S.F. "Reducing Memory Latency in High-Performance Systems" $298,495 June 1994 - Dec 1997
- Intel "Improving the performance of the memory hierarchy" $66,000 + equipment ($64,002) August 1996- July 1999
- NSF "Improving the performance of the memory hierarchy" $340,303 July 1997- Dec 2000
- Intel Corp. "Towards better cache utilization" $82,000 + equipment ($64,002) Jan 1997- July 2000

Selected Recent Publications

1. J.-L. Baer and W.-H.Wang "Multi-Level Cache Hierarchies: Organizations, Protocols and Performance", *Journal of Parallel and Distributed Computing, 6,* 3, 1989 pp.451-476
2. W.-H.Wang, J.-L. Baer, and H.Levy "Organization and Performance of a Virtual-Real Cache Hierarchy" *16th Symp. on Computer Architecture*, June 1989 pp. 140-148
3. H.Mizrahi, J.-L. Baer, E.Lazowska, and J.Zahorjan "Introducing Memory into the Switch Elements of Multiprocessor Interconnection Networks" *16th Symp. on Computer Architecture*, June 1989 pp. 158-166
4. S.-L.Min and J.-L.Baer "A timestamp-based cache coherence scheme" *Proc. Int. Conf. on Parallel Processing,*, 1989, pp.I-29-32
5. S.-L.Min, J.-L.Baer, and H-J.Kim "An Efficient Caching Support for Critical Sections in Large-Scale Shared-Memory Multiprocessors" *Proc., Int. Conf. on Supercomputing* , June 1990, pp.34-47
6. S.-L.Min and J.-L. Baer, "A Performance Comparison of Directory-Based and Timestamped based Cache Coherence Schemes" *Proc. Int. Conf. on Parallel Processing,* 1990, pp. I-305-311
7. J.-L. Baer and R.Zucker "On Synchronization Patterns in Parallel Programs" *Proc. Int. Conf. on Parallel Processing,* 1991, pp.II-60-67
8. W.-H. Wang and J.-L.Baer "Efficient Trace-Driven Simulation Methods for Cache Performance Analysis" *ACM TOCS, 9*, 3 , 1991, pp.222-241 (a revised version of the best paper award in *Proceedings of Sigmetrics* pp. 27-36 May 1990).
9. J.-L. Baer and T.-F. Chen "An Effective On-chip Preloading Scheme to Reduce Data Access Penalty" *Supercomputing 1991* pp.176-186.
10. S.-L.Min and J.-L.Baer " Design and Analysis of a Scalable Cache Coherence Scheme Based on Clocks and Timestamps" *IEEE TPDS, 3* 1, Jan 1992, pp.25-44.

11. R.Zucker and J.-L. Baer "A Performance Study of Memory Consistency Models" *19th Symp. on Computer Architecture*, May 1992 pp. 2-12
12. T.-F.Chen and J.-L. Baer "Reducing Memory Latency via Non-blocking and Prefetching Caches", *Proc. of 5th Int. Conf. on Architectural Support for Programming Languages and Operating Systems*, October 1992, pp.51-61
13. J.Bertoni, J.-L. Baer, and W.-H. Wang "Scaling Shared-Bus Multiprocessors with Multiple Busses and Shared caches" *Microprocessors & Microsystems, 16*, 7, 1992 pp.339-350
14. T.-F.Chen and J.-L. Baer "A Cache Coherence Distributed Directory Scheme for Multiprocessors with Multistage interconnection Networks" *Proc. ICPADS 93*
15. R.Zucker and J.-L. Baer "Software vs. Hardware Coherence: Performance vs. cost" *Proc. 27th Hawaii International Conference on Systems Science*, 1994, I-163-172
16. T.-F.Chen and J.-L. Baer "A Performance Study of Hardware and Software Data Prefetching Schemes" *21st Symp. on Computer Architecture*, April 1994, pp. 223-232
17. X.Qin and J.-L. Baer "A Parallel Trace-driven Simulator: Implementation and Performance" *Proc. Int. Conf. on Parallel Processing,* 1994, pp. II-314-319
18. S.-L.Min, J.Nam, M.Park, and J.-L.Baer "Cache-Based Data Distribution Constrained Scheduling" *Int. Journal of High-Speed Computing*, 6,1, 1994, pp. 139-155
19. C.Anderson and J.-L. Baer "Two Techniques for Improving Performance on Bus-Based Multiprocessors" *Future Generation Computer Systems*, 11, 1995, pp. 537-551 (selected as one of the best papers of *1st Symposium on High-Performance Computer Architecture*, January 1995, pp. 264-275)
20. X.Qin and J.-L.Baer "A comparative study of conservative and optimistic trace-driven simulations" in *28th Annual Simulation Symposium*, (Best paper) April 1995 pp. 42-50
21. T.-F.Chen and J.-L. Baer "Effective Hardware-Based Data Prefetching for High-Performance Processors" *IEEE TC, 44* 11, May 1995 pp. 609-623
22. D.Lee, J.-L.Baer, B. Calder and D.Grunwald "Instruction cache fetch policies for speculative execution" *22nd Symp. on Computer Architecture*, June 1995 pp. 357-367
23. T. Romer, D.Lee, G. Volker, A. Wolman, W. Wong, J.-L. Baer, B. Bershad, and H. Levy "The structure and performance of interpreters", *Proc. of 7th Int. Conf. on Architectural Support for Programming Languages and Operating Systems*, Oct 1996, pp. 150-159
24. X.Qin and J.-L. Baer "On the Use and Performance of Explicit Communication Primitives in Cache-coherent Multiprocessor Systems" *3rd Symposium on High-Performance Computer Architecture*, 1997, pp.182-193
25. X.Qin and J.-L. Baer "A Performance evaluation of cluster-based Architectures", *Proceedings of Sigmetrics*, pp 237-247, 1997.
26. D.Lee, P.Crowley, J.-L. Baer, T.Anderson and B.Bershad "Execution Characteristics of Desktop Applications on Windows NT" *25th Symp. on Computer Architecture*, June 1998 pp. 27-38
27. X.Qin and J.-L. Baer "Optimizing Software Cache-Coherent Cluster Architectures" *Proceedings of SC98* (CD-ROM), Nov 1998
28. D. Lee, J.-L. Baer, B. Bershad and T. Anderson "Reducing Start-up Latency in Web and Desktop Applications", *Proc. 3rd Usenix Windows NT Symposium*, June 1999
29. P. VanVleet, E.Anderson, L.Brown, J.-L. Baer, and A. Karlin "Pursuing the Performance Potential of Dynamic Cache Lines" *Proc. ICCD*, Oct 1999 pp 528-537
30. W.Wong and J.-L.Baer "Modified LRU Policies for Improving Second-level cache Behavior" accepted in *6th Symposium on High-Performance Computer Architecture*, 2000