Chris Diorio

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Research interests

Silicon learning chips, implantable computers, mixed-signal circuit design, ultra–high-speed circuit design.

Education

Years	University	Department	Degree
1992–1997	The California Institute of Technology	Electrical Engineering	Ph.D.
1983–1984	The California Institute of Technology	Electrical Engineering	M.S.
1979–1983	Occidental College	Physics	B.A.

Employment

1997–	Assistant Professor, Computer Science and Engineering, The University of Washington
1992–97	Teaching and Research Assistant, Physics of Computation Laboratory, The California Institute of Technology
1991–97	Senior Staff Engineer, TRW Inc.
1989–91	Senior Staff Scientist, American Systems Corporation
1988–89	Technical Consultant, American Systems Corporation
1986–89	Customer Technical Representative, The Analytic Sciences Corporation
1984–86	Member of the Technical Staff, TRW, Inc.

Honors and awards

2000	An Alfred P. Sloan Foundation Research Fellowship on Feb. 4, 2000.
2000	A Distinguished Lecture Series invitee, the University of Virginia, Department of Computer Science, Jan. 24, 2000. Talk title: "Biologically Inspired Computation".
1999	A Presidential Early Career Award in Science and Engineering (PECASE, sponsored by NSF ECS) on Feb. 10, 1999.
1998	A five-year Packard Foundation Fellowship in Science and Engineering from the David and Lucile Packard Foundation, September, 1998.
1998	An NSF CAREER Award (sponsored by NSF ECS) on May 15, 1998.
1996	The Electron Devices Society's Paul Rappaport Award for the best paper in an IEEE EDS publication during 1996, for "A single-transistor silicon synapse," *IEEE Trans. Electron Devices,* vol. 43, no. 11, pp. 1972–1980, 1996.

Memberships

1988–	The Institute of Electrical and Electronics Engineers

Selected publications

1. M. Figueroa and C. Diorio, "A 200 MHz, 3 mW, 16-tap mixed-signal FIR filter," accepted to Symposium on VLSI Circuits, June, 2000.

2. C. Diorio, "A *p*-channel MOS synapse transistor with self-convergent memory writes," *IEEE Trans. Electron Devices,* vol. 47, no. 2, pp. 464–472, 2000.

3. C. Diorio, T. Humes, H. Notthoff, G. Chao, A. Lai, J. Hyde, M. Kintis, and A. Oki, "A low-noise, GaAs/AlGaAs, microwave frequency-synthesizer IC," *IEEE J. Solid-State Circuits,* vol. 33, no. 9, pp. 1306–1312, 1998.

4. C. Diorio, P. Hasler, B. A. Minch, and C. Mead, "A floating-gate MOS learning array with locally computed weight updates," *IEEE Trans. Electron Devices*, vol. 44, no. 12, pp. 2281–2289, 1997.

5. C. Diorio, P. Hasler, B. A. Minch, and C. Mead, "A complementary pair of four-terminal silicon synapses," *Analog Integrated Circuits and Signal Processing,* vol. 13, no. 1/2, pp. 153–166, 1997.

6. C. Diorio, B. A. Minch, and P. Hasler, "Floating-gate MOS learning systems," *Proc. 1999 Intl. Symp. on the Future of Intellectual Integrated Electronics (ISFIIE),* Sendai, Japan, pp. 515–524, 1999.

7. A. Pesavento, T. Horiuchi, C. Diorio, and C. Koch, "Adaptation of current signals with floating-gate circuits," *Proc. 7th Intl. Conf. on Microelectronics for Neural, Fuzzy, and Bio-Inspired Systems,* Granada, Spain, pp. 128–134, 1999.

8. C. Diorio, P. Hasler, B. A. Minch, and C. Mead, "Hole impact-ionization method of hot-electron injection and four-terminal pFET semiconductor structure for long-term learning," U.S. Patent No. 5,990,512, issued 23 November, 1999.

9. C. Diorio, P. Hasler, B. A. Minch, and C. Mead, "Method for implementing a learning function," U.S. Patent No. 5,914,894, issued 22 June, 1999.

10. C. Diorio and C. Mead, "A *p*MOS analog EEPROM cell," U.S. Patent No. 5,898,613, issued 27 April, 1999.

Graduate students: Miguel Figueroa, Cecilia Hernandez, David Hsu, Matt Richardson, Erik Vee

Undergraduate research students: Dean Brockhausen, Chad Lindhorst, Ryan McDonough, Jeffrey Nichols, Eugene Shih, Adnan Sulejmanpasic, Tim Tuan