

Luis Ceze

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RESEARCH INTERESTS Parallel computer architecture. Also interested in compilation and programming models for parallelism.

EDUCATION ◇ **University of Illinois at Urbana Champaign (UIUC)**, Urbana, IL.
Ph.D. in Computer Science, August 2007 (expected)
Advisor: Josep Torrellas

◇ **University of São Paulo, Polytechnic School**, Brazil.
M.Eng. in Electrical Engineering, August 2002
Thesis: *BGLsim, Complete System Simulator for Blue Gene/L*

◇ **University of São Paulo, Polytechnic School**, Brazil.
B.S. in Electrical Engineering, December 2000

AWARDS AND HONORS ◇ **2007** Ross J. Martin Award, UIUC
· Given by the College of Engineering to recognize outstanding research achievement

◇ **2006** CW Gear Outstanding Graduate Student Award, UIUC
· Given by the CS Department to one outstanding graduate student each year

◇ **2005** Paper selected for the IEEE Micro Top Picks in Computer Architecture, Jan/Feb 2006

◇ **2005** WJ Poppelbaum Memorial Award, UIUC
· For academic merit and creativity in computer architecture

◇ **2005** IBM PhD Fellowship

◇ **2004** IBM Outstanding Internship Award

◇ **2004** IBM PhD Fellowship

◇ **2003** Distinguished Paper, EuroPar 2003

◇ **2003** Top 3 paper in the Fourth LCI International Conference on Linux Clusters

◇ **2002** IBM Bravo! Award for the contribution to the Blue Gene/L project.

PUBLICATIONS REDUCING COMPLEXITY

1. **Luis Ceze**, James Tuck, Pablo Montesinos, Josep Torrellas, "*Bulk Enforcement of Sequential Consistency*", International Symposium on Computer Architecture (**ISCA**), June 2007.
2. James Tuck, **Luis Ceze**, Josep Torrellas, "*Scalable Cache Miss Handling for High Memory-Level Parallelism*", International Symposium on Microarchitecture (**MICRO**), December 2006.
3. **Luis Ceze**, James Tuck, Călin Cașcaval, Josep Torrellas, "*Bulk Disambiguation of Speculative Threads in Multiprocessors*", International Symposium on Computer Architecture (**ISCA**), June 2006.
4. **Luis Ceze**, Karin Strauss, James Tuck, Jose Renau and Josep Torrellas, "*CAVA: Using Checkpoint-Assisted Value Prediction to Hide L2 Misses*", ACM Transactions on Architecture and Code Optimization (**TACO**), June 2006.

5. **Luis Ceze**, James Tuck, Josep Torrellas, “*Are We Ready for High Memory-Level Parallelism?*”, Workshop on Memory Performance Issues (**WMPI** held with HPCA), February 2006. Also appears in ACM SIGMICRO Newsletter, Volume 24, Number 1, April 2006.
6. **Luis Ceze**, Karin Strauss, James Tuck, Jose Renau, Josep Torrellas, “*CAVA: Hiding L2 Misses with Checkpoint-Assisted Value Prediction*”, IEEE Computer Architecture Letters (**CAL**), December 2004.

ARCHITECTURES, COMPILATION AND MODELS FOR PROGRAMMABILITY

7. **Luis Ceze**, Pablo Montesinos, Christoph von Praun, Josep Torrellas, “*Colorama: Architectural Support for Data-Centric Synchronization*”, International Symposium on High Performance Computer Architecture (**HPCA**), February 2007.
8. Christoph von Praun, **Luis Ceze**, Călin Cașcaval, “*Implicit Parallelism with Ordered Transactions*”, Symposium on Principles and Practice of Parallel Programming (**PPoPP**), March 2007.
9. Wei Liu, James Tuck, **Luis Ceze**, Wonsun Ahn, Karin Strauss, Jose Renau, Josep Torrellas, “*POSH: A TLS Compiler that Exploits Program Structure*”, Symposium on Principles and Practice of Parallel Programming (**PPoPP**), March 2006.
10. Jose Renau, Karin Strauss, **Luis Ceze**, Smruti Sarangi, James Tuck, Wei Liu, Josep Torrellas, “*Energy-Efficient Thread-Level Speculation on a CMP*”, IEEE Micro **Top Picks** in Computer Architecture, January/February 2006 issue.
11. Wei Liu, James Tuck, **Luis Ceze**, Karin Strauss, Jose Renau, and Josep Torrellas, “*POSH: A Profiler-Enhanced TLS Compiler that Leverages Program Structure*”, Watson Conference on Interaction between Architecture, Circuits, and Compilers (**P=AC²**), September 2005.
12. Jose Renau, James Tuck, **Luis Ceze**, Karin Strauss, Wei Liu, Josep Torrellas, “*Tasking with Out-of-Order Spawn in TLS Chip Multiprocessors: Microarchitecture and Compilation*”, International Conference on Supercomputing (**ICS**), June 2005.
13. Jose Renau, Karin Strauss, **Luis Ceze**, Smruti Sarangi, James Tuck, Wei Liu, Josep Torrellas, “*Thread-Level Speculation on a CMP Can Be Energy Efficient*”, International Conference on Supercomputing (**ICS**), June 2005.

BLUE GENE AND OTHER

14. George Almasi, Ralph Bellofatto, Jose Brunheroto, Călin Cașcaval, Jose G. Castanos, **Luis Ceze**, Paul Crumley, C. Christopher Erway, Derek Lieber, Xavier Martorell, Jose E. Moreira, Ramendra K. Sahoo, Alda Sanomiya, Karin Strauss, “*An Overview of the Blue Gene/L System Software Organization*”, European Conference on Parallel and Distributed Computing (**EuroPar**), August 2003. (Also appears in Parallel Processing Letters (**PPL**), December 2003).
15. **Luis Ceze**, Karin Strauss, George Almasi, Patrick J. Bohrer, Jose R. Brunheroto, Calin Cascaval, Jose G. Castanos, Derek Lieber, Xavier Martorell, Jose E. Moreira, Alda Sanomiya, Eugen Schenfeld, “*Full Circle: Simulating Linux Clusters on Linux Clusters*”, LCI International Conference on Linux Clusters (**CWCE**), June 2003.
16. **Luis Ceze**, “*BGLsim: Complete System Simulator for Blue Gene/L*”, Masters thesis, University of São Paulo. São Paulo, Brazil, August 2002.
17. Narasimha R. Adiga, George Almasi and others, “*An Overview of the Blue Gene/L Supercomputer*”, International Conference on High Performance Networking and Computing (**SC**), November 2002.
18. George Almasi, George S. Almasi and others, “*Blue Gene/L, a System-on-a-Chip*”, International Conference on Cluster Computing (**CC**), September 2002.

19. Călin Caşcaval, Jose G. Castanos, **Luis Ceze**, Monty Denneau, Manish Gupta and others. “*Evaluation of a Multithreaded Architecture for Cellular Computing*”, International Symposium on High Performance Computer Architecture (**HPCA**), February 2002.
20. George Almasi, George S. Almasi and others, “*Cellular Supercomputing with System-on-a-Chip*”, International Solid State Circuits Conference (**ISSCC**), February 2002.
21. Itana Stiubiener, **Luis Ceze**, Karin Strauss and others, “*An Environment for Easy Cross Synchronization of Multimedia Web Based Material*”, ASEE/IEEE Frontiers in Education (**FIE**), October 2000.

- PATENTS
- ◇ **Luis Ceze** and Călin Caşcaval, “*Method and Apparatus for Implementing Efficient Data Dependence Tracking for Multiprocessor Architectures*”, Patent filed September 2006.
 - ◇ **Luis Ceze**, Erik Altman, Călin Caşcaval, Vijayalakshimi Srinivasan, “*Method and Apparatus for Detection and Recovery of Transient Errors Using SIMD Units*”, Patent filed February 2005.
 - ◇ **Luis Ceze**, Pedro Mindlin, Karin Strauss, “*Smart Board Implementation Using Laser Beam Scanning*”, Patent filed in Brazil, March 2001.
 - ◇ 3 other patent applications on programmability of multiprocessors under preparation. Titles are confidential.

- OTHER
- ◇ Co-author in the proposal “*Novel Programming Model and Architectures to Simplify Parallel Programming*”, January 2007. NSF. Pending.

- RESEARCH EXPERIENCE
- ◇ **Research Assistant**, I-Acoma Group, UIUC (August 2002 – present)
Advisor: Josep Torrellas

My work has centered on parallel computer architecture designs to improve the programmability of parallel machines while reducing their hardware complexity.

To reduce the complexity of multiprocessors, I proposed the *Bulk* architecture, which combines operations on sets of addresses into a few well-defined hardware primitives. I have applied Bulk to maintain coherence and ordering among threads (ISCA'06) and to support sequential memory consistency inexpensively (ISCA'07). To reduce implementation complexity, I also proposed the design of the core (TACO'06, CAL'05) and the memory hierarchy (MICRO'06, WMPI'06) of the CAVA checkpointed processor architecture.

To improve the programmability of multiprocessors, I proposed the *Colorama* architecture (HPCA'07), which associates concurrency control constraints with data — a data-centric approach, in contrast to the traditional code-centric approach of locks and transactions. I also worked extensively on multiple aspects of Thread-Level Speculation (TLS) architectures, including their programming model (PPoPP'07), compiler support (PPoPP'06, PAC2'05), low-power design (ICS'05b, TopPicks'06), and architecture (ICS'05a).

My research on *Bulk* has spurred thesis topics for other students and in other institutions.

- ◇ **Grad Summer Intern**, Programming Models and Tools for Scalable Systems Group. IBM T.J. Watson Research Center. (Summer 2006)
Mentor: Călin Caşcaval and Martin Ohmacht.

I worked on evaluating the potential for using TLS to simplify the manual parallelization of complex applications. As part of the study, I led the design and wrote most of the code of a task recommendation and evaluation tool. This tool, based on binary instrumentation, identifies and reports to the programmer potential places in the program where speculative parallelism may be profitable. The study also resulted in a programming model that exposes speculation features to the programmer (PPoPP'07). The tool is now being used

at IBM to evaluate other task selection algorithms and architectural features.

- ◇ **Grad Summer Intern**, High Performance Programming Environments Group, IBM T.J. Watson Research Center.
(Summer 2004)
Mentor: Călin Cașcaval.

I worked on the Assist Threads effort of the PERCS Project. My work had two main themes: architecture/compilation for TLS and support for efficient redundant computation for reliability. As a result, two invention disclosures were filed: one on reducing the complexity of data dependence violation detection in TLS and one on using SIMD units for redundant computation. In addition, I implemented a generic framework in IBM's TPO (Toronto Portable Optimizer) to support slicing. I received an IBM Outstanding Internship Award.

- ◇ **Grad Summer Intern**, Multithreaded Architectures and Blue Gene Systems Software Group, IBM T.J. Watson Research Center.
(Summer 2003)
Mentors: Monty Denneau and Jose Castaños.

I contributed to two projects: Blue Gene/L and Cyclops64. For the Blue Gene/L, I contributed to the control system of the machine, which is responsible for managing the state of thousands of nodes and also for launching jobs on the processors. For the Cyclops64 project, I evaluated the suitability of new instructions for large integer arithmetic in the Cyclops64 massively multithreaded processor.

- ◇ **Co-op Pre-Professional Engineer**, Blue Gene Systems Software Group, IBM T.J. Watson Research Center.
(June 2001 – July 2002)
Mentor: Jose Moreira.

I contributed to the Blue Gene/C machine (based on the Cyclops processor) by evaluating the memory system (HPCA'02). I also worked on the Blue Gene/L project. I was the main contributor to the Blue Gene/L complete system simulator, BGLsim (CWCE'03). BGLsim was instrumental for the Blue Gene/L system software development. I received the IBM Bravo! Award for the contributions to BGLsim.

- ◇ **Research Assistant** (undergrad, then grad), Computer Architecture and Networks Laboratory, University of São Paulo.
(August 1999 – June 2001)
- ◇ **Research Assistant**, Open Systems Laboratory, University of São Paulo.
(September 1998 – July 1999)

TEACHING EXPERIENCE ◇ **Teaching Assistant**,
CS Department, UIUC
(Spring 2005) CS533: *Parallel Computer Architecture*. Advanced graduate course, with about 30 students.

- ◇ **Cisco Networking Academy Instructor**,
Computer Architecture and Networks Laboratory, University of São Paulo.
(September 2000 – December 2000)

SERVICE Maintainer of SESC, a cycle-accurate multiprocessor simulator (sesc.sourceforge.net).
Member of Technical Staff, Networld+Interop, Las Vegas (2001).

Cisco Certified Academy Instructor (2000).

Cisco Networking Academy, Cisco Certified Network Associate (1999 – 2000).

Helped organize the Computer Architecture Reading Group at the CS Department, UIUC.

Paper Reviewer for MICRO, ISCA, HPCA, P=ac2, PPOPP, PLDI, LCPC, CAL, TACO and Journal of Parallel Computing.

Member of ACM and IEEE.

STATUS Citizen of Brazil, holding an F-1 visa.

- REFERENCES
- ◇ **Prof. Josep Torrellas**, UIUC
torrellas@cs.uiuc.edu
 - ◇ **Prof. Wen-mei Hwu**, UIUC
hwu@crhc.uiuc.edu
 - ◇ **Prof. David Padua**, UIUC
padua@uiuc.edu
 - ◇ **Prof. Sarita Adve**, UIUC
sadve@cs.uiuc.edu
 - ◇ **Prof. Marc Snir**, UIUC
snir@cs.uiuc.edu
 - ◇ **Prof. Craig Zilles**, UIUC
zilles@cs.uiuc.edu
 - ◇ **Dr. Călin Cașcaval**, IBM Research
cascaval@us.ibm.com
 - ◇ **Dr. Jose Moreira**, IBM Research
jmoreira@us.ibm.com
 - ◇ **Dr. Christoph von Praun**, IBM Research
praun@us.ibm.com