

# Jacob Nelson

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## Research

I am interested in using language, runtime, and hardware innovations to better exploit parallel processors.

I am currently working on runtime support for improving performance on large irregular graph problems.

## Publications

*Crunching Large Graphs on Commodity Processors.* Jacob Nelson, Brandon Myers, A.H. Hunter, Luis Ceze, Dan Grossman, Mark Oskin, Carl Ebeling, Simon Kahan, Preston Briggs. 3rd USENIX Workshop on Hot Topics in Parallelism (to appear at HotPar '11), May 2011.

*RCDC: A Relaxed-Consistency Deterministic Computer.* Joseph Devietti, Jacob Nelson, Tom Bergan, Luis Ceze and Dan Grossman. International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS '11), March 2011.

*Dynamic Concurrency Discovery for Very Large Windows of Execution.* Jacob Nelson, Luis Ceze. Workshop on Parallel Execution of Sequential Programs on Multicore Architectures (PESPMA '09), held in conjunction with ISCA '09, June 2009.

## Work Experience

### Google: Summer 2010 to present, Intern

- Performance analysis of virtualization infrastructure

### Cray: Summer 2009, Intern

- Added runtime support for performance profiling to new parallel language Chapel
- Used C++, Chapel, GASNet, Cray XTs

### Google: Summer 2007, Summer 2008, Intern

- Developed microarchitecture, logic, PCB for prototype hardware
- Used Bluespec, Verilog, Haskell, Python, Xilinx FPGAs

### Amazon.com: 2005–2006, Software Development Engineer

- Implemented shipment optimization system based on Ping Xu's Ph.D. thesis at MIT
- Fixed bugs in legacy code; wrote reporting tools; debugged critical operational issues
- Used Java, C++, SQL, Perl, shell scripts, Haskell

### XKL LLC: 2001–2004, Member Technical Staff, Hardware

Processor architect at Cisco Systems founder's high-speed next-generation networking company

- Created PDP-10-like embedded microcontroller, making new product possible

- Reimplemented legacy PDP-10 processor microarchitecture; developed new execution units, microcode, tests
- Negotiated architecture optimizations with compiler team and OS team
- Created environment for test-driven development of CPU
- Designed three processor boards; drove one from concept to fabrication in six weeks (12 signal layers, 5000 nets, 133MHz/2.5GHz)
- Used VHDL, Perl, shell scripts, C, Lisp, PDP-10 assembly, Xilinx FPGAs
- Led system administration team, CPU team

#### **Pacific Northwest National Laboratory: Summer 1999, Intern**

- Set up and tested prototype framebuffer for IBM SP supercomputer
- Used C with MPI, OpenMP

## **Education**

#### **University of Washington, 2006–present**

Computer science Ph.D. student focused on making parallel computers easier to exploit

#### **Pacific Lutheran University, 1996–2000**

B.S. in computer engineering and math, Cum Laude, with Honors

## **Teaching**

Won Bob Bandes Memorial Award for Excellence in Teaching, 2007–2008

#### **Digital design (graduate and undergraduate)**

- Supported student development of a simple 3D rendering pipeline for Professor Mark Oskin's class, Fall 2007
- Implemented BT.601/BT.656-format video processing pipeline for Professor Carl Ebeling's classes, Fall 2006 and Winter 2007

#### **Computer architecture**

- Beginning undergrad version with Professors Mark Oskin, Larry Snyder, Ruth Anderson, Luis Ceze, 2007–2010
- Advanced undergrad version with Professors Jean-Loup Baer and Susan Eggers, Spring 2007
- Co-taught with Professor Tosh Kakar at Pacific Lutheran University in Spring 2006

## **Other**

- Pacific Lutheran University Industrial Advisory Board member
- Winning paper in COMAP's international Mathematical Contest in Modeling, 1999