

#### Modifications to the Xess XS40 Board for Spring 1999:

1. Addition of the Atmel 89C55 uPC (20k flash program memory on chip). This chip has a synchronous reset, so special reset circuitry is needed. It turns out that this chip pulls all ports (P0-P3) low when in the powerup state. Pin 43 on the Atmel (P0.0) is connected to pin 41 (Init) on the Xilinx chip. It turns out that this pin (Init) will halt the Xilinx configuration process while it is held low. Now since the Atmel's reset is synchronous and a programmed Xilinx chip provides the clock to the Atmel, we need to find a way to break this cycle. Our solution was to wire up a LED to pin 41 on the Xilinx chip to monitor the all important signal Init signal, and to wire up a switch to pin 37 on the Xilinx to provide a fake clock. After numerous (usually 10 or so) pushes of the switch, the Atmel will reset. You can finally program the Xilinx successfully. We used a 110 ohm resistor with the LED to power, and a 10 ohm resistor with the switch to power.
2. Addition of the Winbond W241024A SRAM (128k sram – 15ns). This sram has four more pins than the original SRAM on the Xess board (W24257A 32K). One of these pins is a no connect, one is a new enable, and the other two are address bits A15 & A16. We connected A15 to Xilinx pin 30, and A16 to Xilinx pin 72.
3. Dongles used to cut parallel port pins. The standard model was to cut pins D2-D7 and S3-S7. For groups that need Xsram, only pins D4-D7 and S3, S4 & S7 are cut.
4. Addition of a faster clock – 24Mhz. The standard pin used was pin 28. This pin does not work when using a uPC that uses its external data bus (P0 & P2).