CONTINUOUS-TIME FEEDBACK IN FLOATING-GATE MOS CIRCUITS

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ABSTRACT

We present the negative- and positive-feedback circuit configurations of continuous-time floating-gate MOS circuits. We start by reviewing the dynamics of our pFET and nFET single-transistor synapses. We present the range of possible stabilizing and destabilizing types of feedback in circuits with one floating-gate synapse, including data from nFET and pFET synapses. We then show examples of competitive and cooperative behavior in multiple-synapse circuits. We present experimental data from circuits fabricated in the 2μm nwell Orbit CMOS process available through MOSIS.

One of our fundamental requirements of a silicon synapse [1-3] is that the synapse locally implements a learning rule for modifying the weight on the floating gate; in our case, the form of this rule depends on how various error signals are fed back to the floating gate synapse. The nature of this feedback is the focus of this paper. The usefulness of negative or positive feedback depends on the application; Hebbian learning, for example, is a case of destabilizing positive feedback.

This paper considers the behaviors that emerge when single-transistor synapses are coupled together to form various continuous-time learning networks. Our purpose is to understand the dynamics of the learning mechanisms naturally available in floating-gate MOS circuits. We present a deeper discussion of floating-gate dynamics elsewhere [2]. We present experimental data from circuits fabricated in the 2μm nwell Orbit CMOS process available through MOSIS. We have characterized and modeled the dynamics of nFET and pFET single-transistor synapses operating in continuous-time circuits. This work builds the framework to consider floating-gate circuits not only as memory elements, but as continuous-time circuit elements computing at several timescales.

1. MODEL OF SINGLE-TRANSISTOR SYNAPSES

Figure 1 shows circuit diagrams of the nFET and pFET synapses. The starting point is our models of the channel current, electron-tunneling current, and hot-electron–injection current of nFET and pFET floating-gate synapses [1, 2, 3]. For this paper, we define the weight of the synapse, W, as the source current normalized by a bias current, I_{so}. Often we define W without the changes in the floating-gate voltage due input signals at shorter timescales than these

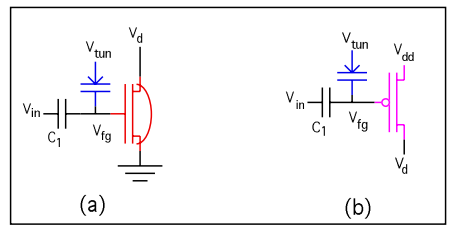

Figure 1: (a) Circuit diagram and small-signal model of the nFET single-transistor synapse with its source connected to ground. (b) Circuit diagram and small-signal model of the pFET single-transistor synapse with its source connected to V_{dd}. For our discussion, we will assume non-negligable levels of electron-tunneling and hot-electron-injection current in these nFET and pFET transistors.

adaptation behaviors [2]. For this paper, we will only model that the input (V_{in}) capacitively couples to V_{fg}, and that the input will change instantanously the floating-gate or drain voltages depending upon the particular circuit. We model the weight dynamics of an nFET synapse as

$$\frac{U_T C_T}{\kappa I_{tun0}}\frac{dW}{dt} = \frac{U_T C_2 W}{\kappa I_{tun0}}\frac{dV_d}{dt} + W^{1-\frac{U_T}{\kappa_n V_x}} - W^{1+\alpha} e^{\Delta V_d / V_{inj}}, \tag{1}$$

and we model the weight dynamics of a pFET synapse as

$$-\frac{U_T C_T}{\kappa I_{tun0}}\frac{dW}{dt} = \frac{U_T C_2 W}{\kappa I_{tun0}}\frac{dV_d}{dt} + W^{1+\frac{U_T}{\kappa_p V_x}} - W^{1+\alpha} e^{-\Delta V_d / V_{inj}}. \tag{2}$$

We define C_T as the total amount of capacitance connected to the floating gate, V_x as a tunneling parameter related to the quiescent tunneling and floating-gate voltages, V_{inj} as an injection parameter related to the quiescent drain and floating-gate voltages, I_{tun0} as the quiescent tunneling and injection current, which is primarily dependant upon the tunneling voltage and power-supply voltage, α as $1 - \frac{U_T}{V_{inj}}$, and C_2 as the capacitance between floating gate and drain (which is not explicitly drawn for clarity). We assume that all the floating-gate devices are matched. A typical nFET value of α is 0.70, and a typical pFET value of α is 0.90; both values are consistent with typical values of V_{inj}. For our operating conditions, a typical value of V_x is $1V$ with the 42nm oxide used in the 2.0μm Orbit process.

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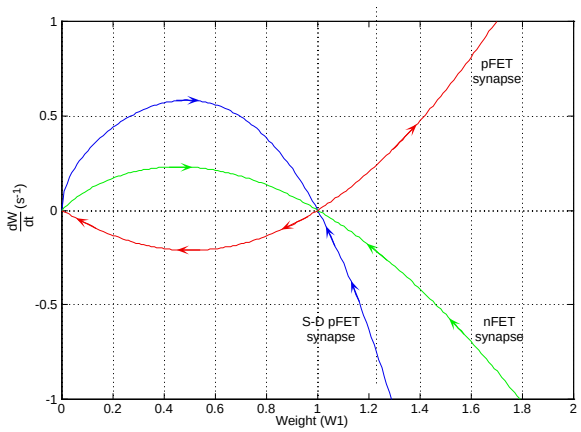

Figure 2: Plot of the time-derivative of W versus W for the nFET, and pFET synapses. The arrows show the direction that the differential equation will take. This figure shows that the nFET synapse will stabilize to the $W = 1$ steady state, while the pFET synapse will diverge from the $W = 1$ steady state.

Figure 2 graphs (1) and (2) for a fixed input and drain voltage for typical parameter values. In previous discussions, we plotted experimental data of $\frac{dW}{dt}$ versus W either only for tunneling current or only for injection current [2, 1]; this curve is a combination of our previous plots. We see that the $W = 1$ equilibrium for the nFET synapse is stable, but that the $W = 1$ equilibrium for the pFET synapse is unstable.

2. DYNAMICS OF SINGLE-SYNAPSE CIRCUITS

We wil illustrate the basic floating-gate feedback mechanisms by considering the class of circuits composed of one synapse. We will restrict our discussion to synapse dynamics that depend only on the drain and floating-gate terminals; similar feedback mechanisms occur with other configurations that employ various combinations of the drain, source, and tunneling terminals.

The dynamic behavior of a single synapse can be characterized from that synapse's response in both a constant-current configuration and a constant-voltage configuration. Figure 3 shows the pFET and nFET circuits comprising a single synapse: first the circuits with the the drain connected to a current source, and second the circuits with the drain connected to a cascode transistor. We assume that the synapses have nonnegligible tunneling and injection currents. Figure 3 shows the pFET and nFET circuit responses to an upgoing and downgoing input step. For a pFET synapse, the constant-current configuration is stable, because the type of floating-gate feedback from its drain is stable. The autozeroing floating-gate amplifier (AFGA) is based on the stability of this configuration [4]. For an nFET synapse, the constant-voltage configuration is stable, because the type of floating-gate feedback from its floating gate is stable. The pFET synapse's constant-voltage configuration and the nFET-synapse's constant-current configuration are unstable circuits. For all four circuits, equilibrium is established when the tunneling current is balanced by the injection current.

The condition that sets the boundary between the stable and unstable regimes occurs when a particular load resistance, R_l, is connected to the transistor's drain terminal. The condition for the pFET and nFET synapses is

$$\text{nFET} : R_l g_m = \frac{U_T/\kappa_p || V_x}{V_{inj}},$$

$$\text{pFET} : R_l g_m = \frac{U_T/\kappa_p || -V_x}{V_{inj}}, \qquad (3)$$

where we define $x||y$ as $\frac{xy}{x+y}$, and g_m is the transconductance of the nFET or pFET transistor. Because this formulation is valid for positive and negative resistances connected to the drain, negative drain resistance is stablizing for nFETs and destabilizing for pFETs.

From (1) and (2), we can analyticaly predict the behaviors in Fig. 3. First, consider the nFET and pFET circuits in the constant-current configuration. In both cases, the source current is fixed at I_{so} (W = 1), and the tunneling current is held constant at I_{tun0} because of the constant floating-gate voltage. Using these simplifications results in the model:

$$\text{nFET} : C_2 \frac{dV_{out}}{dt} = I_{tun0} \left(e^{\Delta V_{out}/V_{inj}} - 1 \right),$$

$$\text{pFET} : C_2 \frac{dV_{out}}{dt} = I_{tun0} \left(e^{-\Delta V_{out}/V_{inj}} - 1 \right). \qquad (4)$$

In the case of the AFGA, we previously showed that equations of this form can be solved analytically [4]. The trajectories of the pFET equation converge to the steady state at $\Delta V_{out} = 0$, but the trajectories of the nFET equation diverge away from the steady state at $\Delta V_{out} = 0$.

Second, consider the nFET and pFET circuits in the constant-voltage configuration. Because the drain voltage of the pFET and nFET synapses are fixed by the cascode transistor, we simplify (1) and (2) to

$$\text{pFET} : \frac{C_T U_T}{\kappa_p I_{tun0}} \frac{dW}{dt} = -W^{1+\frac{U_T}{\kappa_p V_x}} + W^{1+\alpha},$$

$$\text{nFET} : \frac{C_T U_T}{\kappa_n I_{tun0}} \frac{dW}{dt} = W^{1-\frac{U_T}{\kappa_n V_x}} - W^{1+\alpha}. \qquad (5)$$

We can easily see the dynamics by rewriting these equations as

$$\text{nFET} : \frac{C_T U_T}{\kappa_n I_{tun0}} \frac{dW_1}{dt} = W_1^{1-\frac{U_T}{\kappa_n V_x}} \left(1 - W_1^{1+\frac{U_T}{\kappa_n (V_x || -V_{inj})}} \right),$$

$$\text{pFET} : \frac{C_T U_T}{\kappa_p I_{tun0}} \frac{dW_1}{dt} = W_1^{1+\frac{U_T}{\kappa_p V_x}} \left(W_1^{\alpha-\frac{U_T}{\kappa_p V_x}} - 1 \right). \qquad (6)$$

As in the fixed channel-current case, these two equations are very similar. The trajectories of the nFET differential equation converge toward $W = 1$ and diverge away from $W = 0$, but the trajectories of the pFET differential equation converge toward $W = 0$ and diverge away from $W = 1$. We call the nFET circuit an autozeroing transconductance amplifier, because the output current always returns to the same equilibrium level.

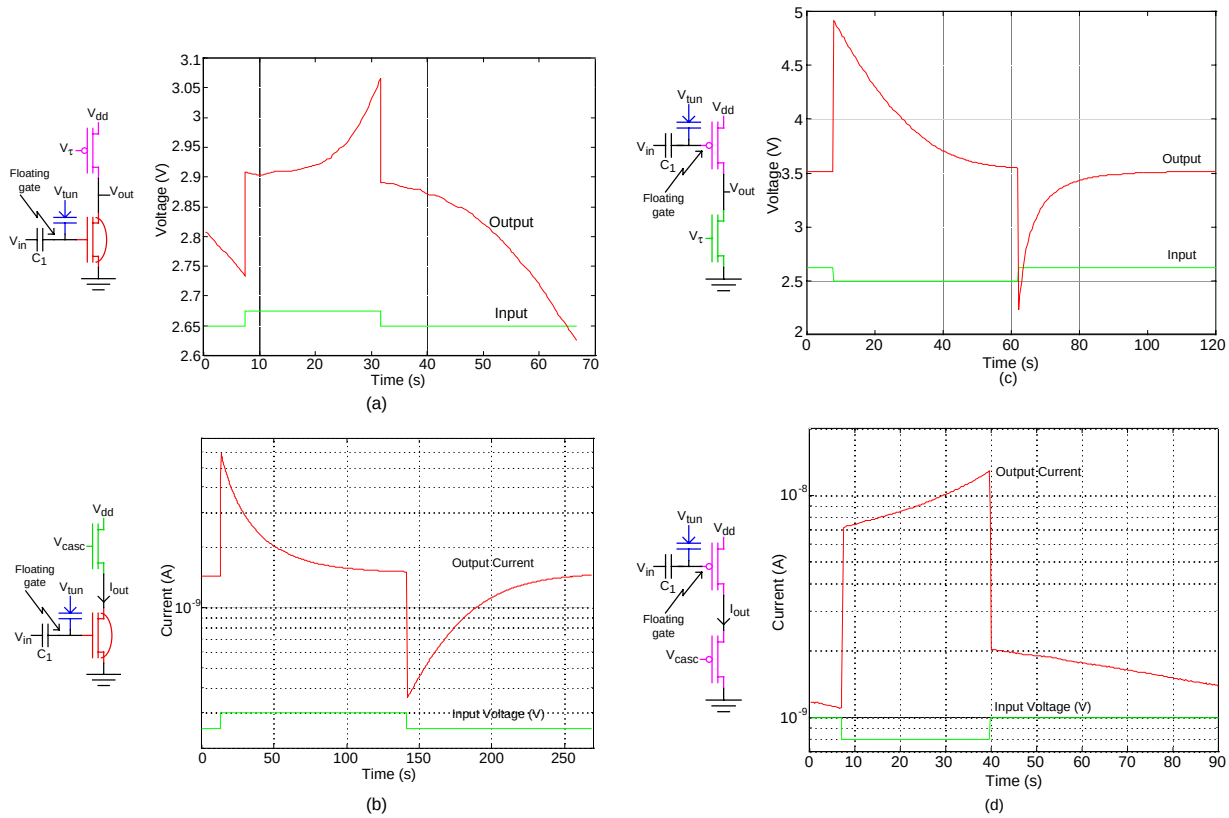

Figure 3: Experimental measurements of dynamics fo circuits comprising a single nFET or pFET synapse. (a) The nFET voltage-adapting circuit configuration and its response to an upgoing and downgoing step input. The circuit configuration is unstable. (b) The nFET current-adapting circuit configuration and its response to an upgoing and downgoing step input. The circuit configuration is stable. (c) The pFET voltage-adapting circuit configuration, and its response to an upgoing and downgoing step input. This circuit is the autozeroing floating-gate amplifier (AFGA). The adaptation in response to an upward step results from electron tunneling; the adaptation in response to a downward step results from pFET hot-electron injection. This amplifier had a gain of 11.2, and I_{tun0} is $50fA$. (d) The pFET current-adapting circuit configuration, and its response to an upgoing and downgoing step input. The circuit configuration is unstable.

3. NETWORKS OF TWO COUPLED SYNAPSES

This section considers the interaction of two synapses coupled though their drain terminals. Figure 4 shows the circuits with two coupled nFET synapses and with two coupled pFET synapses. We consider only the stable circuit configurations from the previous section, because it is difficult to illustrate the behavior of circuits that have no stable operating point. The nFET synapses are constrained by the cascode transistor. The two nFET synapses cooperate for the entire available channel current; regardless of the starting position, the two synapses converge to nearly equal channel currents. The pFET synapse channel currents are constrained by a current source, which we define to be the sum of the bias currents in each synapse. The two pFET synapses compete for the available bias current; the synapse starting with the larger channel current will eventually supply all the bias current. These properties extend directly to multiple synapses.

The output voltage (V_{out}) in both circuits returns to its equilibrium value. If we model each synapse by (1) or (2) and add the two equations for the two synapse weights (W_1 and W_2), we get equations which model the output voltage behavior as

$$\text{nFET}: \frac{C_T + \kappa_n C_2}{\kappa_n I_{tun0}} \frac{dV_{out}}{dt} = B_1 - Ae^{\frac{\Delta V_{out}}{V_{inj}}}.$$

$$\text{pFET}: \frac{C_2}{I_{tun0}} \frac{dV_{out}}{dt} = Ae^{-\frac{\Delta V_{out}}{V_{inj}}} - B_2, \qquad (7)$$

where $A = W_1^{1+\alpha} + W_2^{1+\alpha}$, $B_1 = W_1^{1-\frac{U_T}{\kappa_p V_x}} + W_2^{1-\frac{U_T}{\kappa_p V_x}}$, and $B_2 = W_1^{1+\frac{U_T}{\kappa_p V_x}} + W_2^{1+\frac{U_T}{\kappa_p V_x}}$. A, B_1, and B_2 are always positive and weak functions functions of W_1, W_2; as a result both equations are qualitatively identical to the output-voltage equation of the AFGA. The ΔV_{out} trajectories converge to the circuit's steady state.

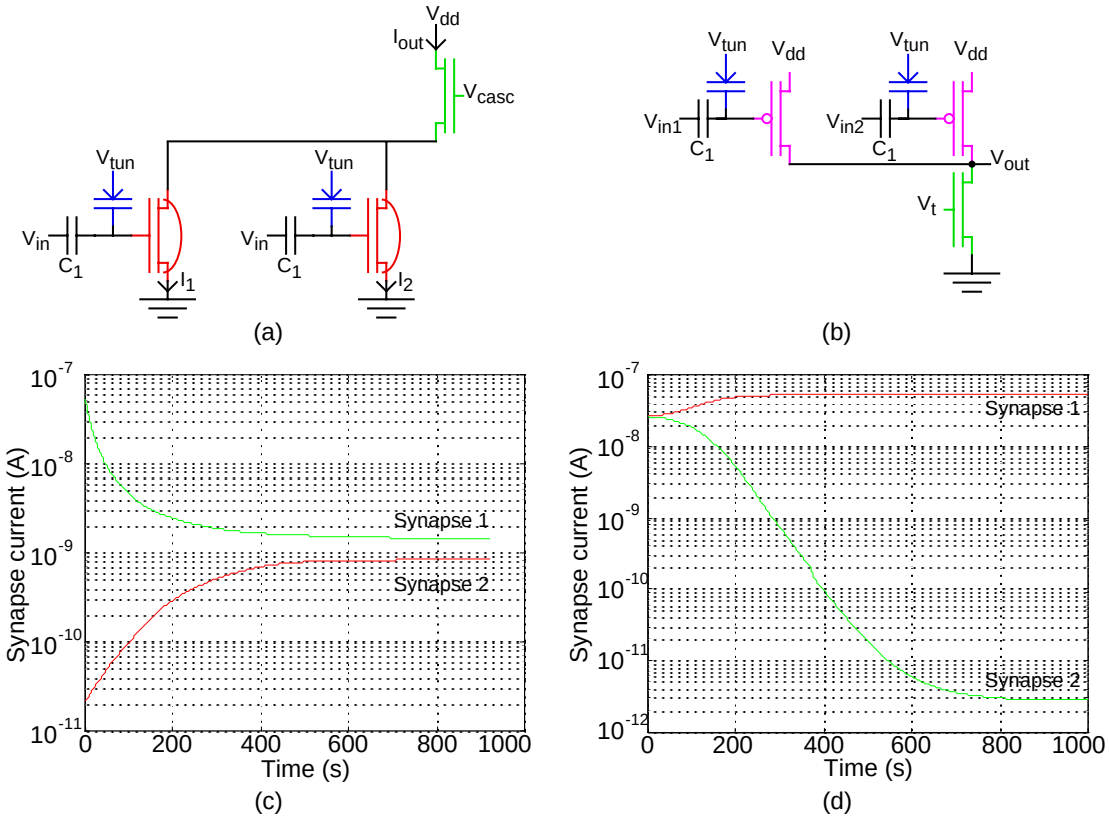

Figure 4: Experimental of the behavior of coupled nFET and pFET synapses for fixed inputs. (a) Circuit of the two nFET synapses coupled at the drain with a cascode transistor. (b) Circuit of the two pFET synapses coupled at the drain with a current source. (c) The synapse current variation with time when the currents initially start far apart from each other. Both currents eventually converge to their steady state levels. (d) The synapse current variation with time when the currents initially start near each other. I_1 wins and I_2 loses, where I_2 decreases as a linear exponential in time due to the constant tunneling current at the floating gate. The measured I_2 saturates due to the surrounding leakage currents; the floating gate continues to increase with time.

Once the output voltage has reached equilibrium, each synapse acts like its corresponding single-synapse circuit with a fixed drain voltage. For the coupled nFET circuit, Fig. 4c shows that, even if the two starting weights are orders of magnitude apart, then, over time, both weights will converge to nearly the same current. This behavior is typical of a continuous-time anti-Hebbian network. A nearly fixed drain voltage means that the synapses are only weakly coupled through the drain; we could achieve stronger coupling with a negative-resistance circuit. For the coupled pFET circuit, Fig. 4d shows that, if the two starting weights are equal, then, over time, one weight will decrease to 0 and the current in the other synapse will be equal to the bias current. If the losing weight is brought slightly above the winning weight, what was the losing synapse will now be the winner. The pFET synapses compete with each other for the bias current; in some sense, we have winner-take-all behavior in the weight space. This behavior is typical of a continuous-time normalizing Hebbian network; after a period of time, we cannot reuse these synapses without significantly altering this circuit.

4. REFERENCES

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