Data Pattern Generator

**Features & Benefits**

- Data Rate to 1.1 Gb/s Tests High-speed Logic Devices and Circuits
- Data Pattern Depth to 256 K/Channel Speeds Characterization
- Multiple Output Channels Increases Flexibility
  - DG2040: 2
  - DG2030: 4 or 8
  - DG2020A: 12, 24, or 36
- Control of Edge Timing (DG2040) Permits Jitter Simulation in Serial Data Streams
- Precise Control of Output Parameters Include:
  - Variable Output Delay
  - Variable Output Level
  - Variable Rise and Fall Time Control (DG2030)
  - Tri-state Output Control (DG2020A, DG2030)
- Fast Transition Times to 150 ps (DG2040) Aids Fast Logic Evaluation
- Complementary Output (DG2040) Assures Excellent Signal Fidelity

**Applications**

- Ultra Low Jitter for Clock Substitution
- Characterized Device Timing for TTL, CMOS, ECL Families
- Simulate Missing Functions in System or Subsystem Evaluation
- Create Complex Data Patterns with Sophisticated Sequence, Looping, Jump on Event and Tri-state Output Control
- Characterize and Verify ASIC, FPGA and DACs
- Test Printer Engines or LCD Display Drivers
- Use in Conjunction with TLA Logic Analyzer to Provide Digital Stimulus

**Choose the Best Fit**

The DG2000 Series is remarkable for its balanced approach to providing the appropriate class of instrument for a wide variety of digital design applications. Performance ranges from 1.1 Gb/s to 200 Mb/s and from 2 to 36 channels. The table illustrates the principal specifications for members of the DG2000 Series.

The DG2000 Series of pattern generators provide digital designers with the high performance tools needed to evaluate advanced digital semiconductors and logic circuits. Whatever you call your design process – characterization, debug, validation or verification – as a digital designer you must have a state-of-the-art digital pattern generation as you push the edge of the technology envelope and race to market.
Data Pattern Generator

The DG2000 Series is the ideal solution for applications where you must characterize device or circuit timing and amplitude margins. The DG2000 Series is perfect for simulating setup and hold violations or conditions of metastability. The DG2000 graphical user interface allows you to quickly create complex data patterns with a few keystrokes on the front panel. Use the advanced sequence editing capability of the DG2000 Series to insert infrequent faults or glitches in your data patterns to verify device or circuit recovery. The DG2000 Series is an invaluable tool, allowing you to simulate missing system functionality while meeting critical market windows. With the introduction of the DG2040, new capabilities are available to control clock and data jitter or modulate pulse edges on a selective basis (Figure 1).

### Critical Timing

The DG2000 Series is the ideal solution for applications where you must characterize device or circuit timing and amplitude margins. The DG2000 Series is perfect for simulating setup and hold violations or conditions of metastability. The DG2000 graphical user interface allows you to quickly create complex data patterns with a few keystrokes on the front panel. Use the advanced sequence editing capability of the DG2000 Series to insert infrequent faults or glitches in your data patterns to verify device or circuit recovery. The DG2000 Series is an invaluable tool, allowing you to simulate missing system functionality while meeting critical market windows. With the introduction of the DG2040, new capabilities are available to control clock and data jitter or modulate pulse edges on a selective basis (Figure 1).

#### DG2000 Series Principal Specifications

<table>
<thead>
<tr>
<th>Feature</th>
<th>DG2040</th>
<th>DG2030</th>
<th>DG2020A</th>
</tr>
</thead>
<tbody>
<tr>
<td>Data Rate</td>
<td>1.1 Gb/s</td>
<td>400 Mb/s</td>
<td>200 Mb/s</td>
</tr>
<tr>
<td>Pattern Depth</td>
<td>256 K/CH.</td>
<td>256 K/CH.</td>
<td>64 K/CH.</td>
</tr>
<tr>
<td>Rise &amp; Fall Time (20% to 80%)</td>
<td>150 ps at 1 Vp-p</td>
<td>1.5 ns at 2.5 Vp-p</td>
<td>2 ns at 5 Vp-p</td>
</tr>
<tr>
<td>No. of Channels</td>
<td>2</td>
<td>4 or 8</td>
<td>12, 24 or 36</td>
</tr>
<tr>
<td>Features</td>
<td>Edge control</td>
<td>Variable tr &amp; tf time</td>
<td>Bus wide testing</td>
</tr>
</tbody>
</table>

![Figure 1](image.png)

**Figure 1.** The DG2040 allows specific edges to be identified and time adjusted or jittered by ±100 ps. An external modulation source can be used to provide continuously variable jitter.
**Characteristics**

### Sequencer
- **Maximum Number of Blocks**: 256.
- **Maximum Number of Sequence Steps**: DG2040: 4000; DG2030: 4000; DG2020A: 2048.
- **Block Repeats Per Line**: 1 to 65536 or infinite.

### Internal Trigger Generator (DG2030, DG2040)
- **Range**: 1.0 µs to 10.0 s.
- **Resolution**: 3 digits, 0.1 µs minimum.
- **Accuracy**: ±0.01%.

### Data and Clock Output (DG2040)
- **Data**
  - **Output**: Standard: CH 0 & CH 1 at front-panel SMA and Clock at rear panel SMA connectors.
  - **Data Rate**: 0.1 b/s to 1100 Mb/s.
  - **Sampling Rate**: 0.1 Hz to 1100 MHz.
  - **Resolution**: 7 digits.
  - **Clock Output Period Jitter**: <30 ps at 1100 MHz, Typical; <50 ps at 200 MHz, Typical.
  - **CH0 Period Jitter (Clock Pattern)**: <20 ps at 1100 MHz, Typical; <200 ps at 400 MHz, Typical.
  - **Accuracy**: PLL On, ±0.0001%; PLL Off, ±3%.
  - **Pattern Depth**: 360 to 256 Kbits (4 increment).
- **Data Width**: 2-Bits (complementary outputs) via front-panel SMA connectors.

### Impedance
- **50 Ω**.

### Rise/Fall Time (20 to 80%)
- **<150 ps at 1 Vp-p and 10 MHz**.

### Delay Function
- **Delay Channel**: CH 0 or CH 1.
- **Delay Time**: –1 ns to +2 ns.
- **Delay Resolution**: 10 ps.
- **Accuracy**: <(±3% of setting) ± | 25 ºC – Ta | * 15 ps ±100 ps (where Ta is the ambient temperature °C).

### Channel Skew
- **(<± | 25 ºC – Ta | *15 ps ±100 ps)** where Ta is the ambient temperature °C.

### Data Pattern Generator
- **www.tektronix.com/signal_sources**

---

**Output Data**

<table>
<thead>
<tr>
<th></th>
<th>DG2040</th>
<th>DG2030</th>
<th>DG2020A</th>
</tr>
</thead>
<tbody>
<tr>
<td>Data Rate</td>
<td>0.1 b/s to 1100 Mb/s</td>
<td>0.1 b/s to 409.6 Mb/s</td>
<td>0.1 b/s to 200 Mb/s</td>
</tr>
<tr>
<td>Sampling Rate</td>
<td>0.1 Hz to 1100 MHz</td>
<td>0.1 Hz to 409.6 MHz</td>
<td>0.1 Hz to 200 MHz</td>
</tr>
<tr>
<td>Resolution</td>
<td>7 digits</td>
<td>7 digits</td>
<td>4 digits</td>
</tr>
<tr>
<td>Clock Output Period Jitter</td>
<td>&lt;30 ps at 1100 MHz, Typical</td>
<td>&lt;50 ps at 200 MHz, Typical</td>
<td>&lt;50 ps at 200 MHz, Typical</td>
</tr>
<tr>
<td>CH0 Period Jitter (Clock Pattern)</td>
<td>&lt;20 ps at 1100 MHz, Typical</td>
<td>&lt;200 ps at 400 MHz, Typical</td>
<td>&lt;35 ps at 200 MHz, Typical</td>
</tr>
<tr>
<td>Accuracy</td>
<td>PLL On, ±0.0001%; PLL Off, ±3%</td>
<td>PLL On, ±0.0001%; PLL Off, ±3%</td>
<td>PLL On, ±0.0005%; PLL Off, ±3%</td>
</tr>
<tr>
<td>Pattern Depth</td>
<td>360 to 256 Kbits (4 increment)</td>
<td>90 to 256 Kbits (1 increment)</td>
<td>64 to 64 Kbits (1 increment)</td>
</tr>
<tr>
<td>Data Width</td>
<td>2-Bits (complementary outputs) via front-panel SMA connectors</td>
<td>Standard: 4-Bits via front-panel BNC connectors Optional: 8-Bits via 4-front-panel, 4 rear-panel BNC connectors</td>
<td>Standard: 12-Bits Optional: 24- or 36-Bits</td>
</tr>
</tbody>
</table>

---

**Data Pattern Generator • DG2040 • DG2030 • DG2020A**
Data Pattern Generator

DG2040 • DG2030 • DG2020A

Data and Clock Output (DG2030)

Data –

Output:
Standard: CH 0 to CH 3 and Clock at front-panel BNC connectors.
Optional: CH 4 to CH 7 at rear-panel BNC connectors.

VOH: –1.25 V to +3.5 V into 50 Ω.
VOL: –1.50 V to +3.25 V into 50 Ω.
Resolution: 5 mV.
Maximum Swing: 5 Vp-p.
Minimum Swing: 250 mVp-p.
Aberration: ≤5% at 3.5 Vp-p.
Impedance: 50 Ω.
Rise/Fall Time (20 to 80%): Variable at amplitude range from 2 Vp-p to 5 Vp-p.
Variable Range: Depends on amplitude setting.
Value in Fast: 0.25 Vp-p to 1 Vp-p; 500 ps.
1.7 ns at 3.00 Vp-p,
Accuracy: ±10% of setting ±500 ps.

Auxiliary Inputs
Clock –
DG2040: Rear-panel BNC connectors (10 MHz reference).
DG2030: Rear-panel BNC connector.
DG2020A: Rear-panel SMB connector.

Frequency:
DG2040: 10 MHz ±0.1 MHz.
DG2030: DC to 409.6 MHz.
DG2020A: DC to 200 MHz.

Input voltage range: 0.2 V to 3.0 Vp-p.
Input voltage level: ±10 Vp-p.
Impedance: 50 Ω, AC coupling.

DG2020A and DG2030 –
Impedance: 50 Ω, terminated to +0.5 V.
Delay to Clock Out: 36 ns (typical).

Trigger –
Front-panel BNC connector.
Level: –5.0 V to +5.0 V.
Resolution: 0.1 V.
Threshold accuracy: ±5% of setting ±0.1 V.
Minimum Pulse Width: ≥10 ns.
Sensitivity: >0.5 Vp-p.
Impedance: 1 kΩ or 50 Ω.

Maximum Input: ±10 V into 1 kΩ, ±5 V into 50 Ω.
Polarity: Positive or negative.
Hold Off:
DG2040: 100 ns minimum.
DG2030: 100 ns minimum.
DG2020A: 500 ns minimum.

Event (DG2040 and DG2030 only) –
Rear-panel BNC connector.
Threshold Level: –5.0 V to +5.0 V.
Resolution: 0.1 V.
Set-up Time to Next Block:
DG2040: 230.5 to 254.5 clocks before the next block.
DG2030: 48 to 53 clocks before the next block.
Polarity: Positive edge.
Minimum Pulse Width: 100 ns.

Inhibit (DG2030 only) –
Rear-panel BNC connector.
Mode:
Off: Always enabled.
Internal: Controlled by CH 0 signal.
External: Controlled by inhibit input signal.
Both: Controlled by CH 0 or inhibit input signal.
Threshold Level: –5.0 V to +5.0 V into 1 kΩ.
Resolution: 0.1 V.
Delay to Data Output: 34 ns to 38 ns (typical).
Delay to Clock Output: 7 ns to 11 ns (typical).

Auxiliary Outputs
Sync –
DG2040: Rear-panel BNC connector.
DG2030: Rear-panel BNC connector.
DG2020A: Front-panel BNC connector.

Level:
2.5 V into 50 Ω.
0 V into 50 Ω.
Pulse Width:
DG2040: 32 to 36 clocks.
DG2030: 9 or 10 clocks.
Impedance: 50 Ω.
**Event**

DG2040: Rear-panel BNC connector.
DG2030: Rear-panel BNC connector.
DG2020A: Front-panel BNC connector.

**Level**

- DG2040: $V_{OH}$, 2.5 V into 50 Ω; $V_{OL}$, 0 V into 50 Ω.
- DG2030: $V_{OH}$, 2.5 V into 50 Ω; $V_{OL}$, 0 V into 50 Ω.
- DG2020A: Positive TTL pulse, 50 Ω.

**Output Term**

- DG2040: 180 to 200 clocks.
- DG2030: 45 to 50 clocks.
- DG2020A: 8 clocks.

**Delay Time**

- DG2040: 194.5 to 214.5 clocks before data output change.
- DG2030: 48 to 53 clocks before data output change.

**Impedance**

50 Ω.

**Clock (DG2020A only)**

- Rear-panel SMB connector.

**Level**

1 V (typical) into 50 Ω.

**Delay From Trigger Input**

PLL On:

- >6.25 MHz: 15 to 40 ns.
- <6.25 MHz: 25 to 60 ns.

PLL Off:

- >6.25 MHz: 15 to 45 ns.
- <6.25 MHz: 25 to 60 ns.

External: 7 ns + 1 clock to 20 ns + 0.5 clock.

**Programmable Interface**

- RS-232-C: 19.2 Kbps, D-sub 9-Pin connector.

---

**P3410 TTL Data Output Pod Characteristics**

**Data Output**

Channels – 12.

**Connector** – 26-Pin header.

$V_{OH}$ – >4.4 V into 1 MΩ.

$V_{OL}$ – >0.1 V into 1 MΩ.

**Rise/Fall Time** – <5 ns into 1 MΩ, 10 pF (20% to 80%).

**Internal Clock Out to Data Delay** – 24 ns.

**External Clock Input to Data Output Delay** – 25 to 45 ns.

**Trigger Input to Data Output Delay**

**Internal Clock**:

- >6.25 MHz: 30 to 65 ns.
- <6.25 MHz: 45 to 80 ns.

**External Clock**:

- 25 ns + 0.5 clock to 45 ns + 1.5 clock.

**Delayed Channels**

Delay Channel – CH 8, CH 9, CH 10, CH 11.

Delay Time – 0 to 20 ns.

Delay Resolution – 0.1 ns.

**Channel Skew**

CH 0 and other channels, same pod: <3 ns.
CH 0 and CH 0, two pods of same type: <2 ns.

---

**Event Input**

Threshold Level – TTL.

**Delay to Data Output** – ≤50 ns + 50 clocks.

**Set-up Time to Next Block** – 47 to 54 clocks.

**Inhibit Input**

**Level** – TTL, 1 kΩ.

**Delay to Data Output** – 18 ns.

**Internal Inhibit Delay** – 5 ns.

---

**Physical Characteristics**

**Dimensions**

<table>
<thead>
<tr>
<th></th>
<th>mm</th>
<th>in.</th>
</tr>
</thead>
<tbody>
<tr>
<td>Height*1</td>
<td>51</td>
<td>2.0</td>
</tr>
<tr>
<td>Width</td>
<td>150</td>
<td>5.9</td>
</tr>
<tr>
<td>Depth</td>
<td>101</td>
<td>4.0</td>
</tr>
<tr>
<td>Weight</td>
<td>kg</td>
<td>lb.</td>
</tr>
<tr>
<td>Net</td>
<td>0.5</td>
<td>1.1</td>
</tr>
</tbody>
</table>

*1 Including feet.
**P3420 Variable Data Output Pod Characteristics**

**Data Output**
- Channels – 12.
- Connector – SMB.
- $V_{OH} = -2.0 \text{ V to } +7.0 \text{ V into } 1 \text{ M} \Omega$.
- $V_{OL} = -3.0 \text{ V to } +6.0 \text{ V into } 1 \text{ M} \Omega$.
- Resolution – 0.1 V.
- Maximum Swing – 9.0 $V_{pp}$.
- Minimum Swing – 0.5 $V_{pp}$.
- Output Current – Total Output Current: <500 mA. Sink: <–30 mA/CH. Source: >+30 mA/CH.
- Rise/Fall Time – <2 ns into 1 MΩ, 10 pF, 5 $V_{pp}$, swing (20% to 80%).
- Internal Clock Out to Data Delay – 20 ns.
- External Clock Input to Data Output Delay – 20 to 40 ns.
- Trigger Input to Data Output Delay – Internal Clock: >6.25 MHz: 30 to 60 ns. <6.25 MHz: 40 to 70 ns.
- Delay Channel – CH 8, CH 9, CH 10, CH 11.
- Delay Time – 0 to 20 ns.
- Delay Resolution – 0.1 ns.
- Channel Skew – CH 0 and other channels, same pod: <3 ns. CH 0 and CH 0, two pods of same type: <2 ns.

**Event Input**
- Threshold Level – –5.0 V to +5.0 V.
- Resolution – 0.1 V.
- Delay to Data Output – ±45 ns ± 50 clock.
- Set-up Time to Next Block – 47 to 54 clocks.

**Inhibit Input**
- Threshold Level – –5.0 V to +5.0 V, 1 kΩ.
- Resolution – 0.1 V.
- Delay to Data Output – 16 ns.
- Internal Inhibit Delay – –2 ns.

**Physical Characteristics**

<table>
<thead>
<tr>
<th>Dimensions</th>
<th>mm</th>
<th>in.</th>
</tr>
</thead>
<tbody>
<tr>
<td>Height*</td>
<td>51</td>
<td>2</td>
</tr>
<tr>
<td>Width</td>
<td>255</td>
<td>10</td>
</tr>
<tr>
<td>Depth</td>
<td>161</td>
<td>6.3</td>
</tr>
<tr>
<td>Weight kg</td>
<td>1</td>
<td>2.2</td>
</tr>
</tbody>
</table>

**Environmental**
- Temperature – Operating: +10 ºC to +40 ºC. Nonoperating: –20 ºC to +60 ºC.
- Humidity – Operating: 20% to 80% (no condensation). Nonoperating: 5% to 30% (no condensation).
- Altitude – Operating: Up to 4.5 km (15,000 ft.). Nonoperating: Up to 15 km (50,000 ft.).
- Vibration – Operating: 0.33 mm p-p, 10 to 55 Hz, 15 minutes.
- Shock – Nonoperating: 294 m/s² (30 g), half-sine, 11 ms duration.

**Certification and Compliance**
- Safety – UL1244, CSA231, EN61010-1, IEC61010-1.

**Power**
- Power Consumption – 300 W maximum.
- Maximum Current – 4 A.

**Physical Characteristics**

<table>
<thead>
<tr>
<th>Dimensions</th>
<th>mm</th>
<th>in.</th>
</tr>
</thead>
<tbody>
<tr>
<td>Height*</td>
<td>164</td>
<td>6.4</td>
</tr>
<tr>
<td>Width*</td>
<td>362</td>
<td>14.3</td>
</tr>
<tr>
<td>Depth*</td>
<td>491</td>
<td>8.25</td>
</tr>
<tr>
<td>Weight kg</td>
<td>9.7</td>
<td>21.4</td>
</tr>
</tbody>
</table>

* Including feet.
** Including handle.
* Including front cover. 576 mm (22.2 in.) with handle extended.

Characteristics shown are typical. Please refer to individual product user manuals for complete specifications.
Data Pattern Generator

DG2040
Data Generator.
Please specify power plug when ordering.
Options
Opt. 1R – Rackmount. Floppy drive access moved to front panel.

DG2030
Data Generator.
Please specify power plug when ordering.
Options
Opt. 1R – Rackmount. Floppy drive access moved to front panel.
Opt. 01 – Eight-channel output. Adds four-channel output from rear panel.
Opt. 1R – Rackmount. Floppy drive access moved to front panel.

DG2020A
Data Generator.
Please specify power plug when ordering.
Options
Opt. 01 – Adds a 12-Bit digital port for a total of 24 output channels. Includes pod connection cables (174-3548-00). Order P3410 or P3420 pod separately.
Opt. 02 – Adds two 12-Bit digital ports for a total of 36 output channels. Includes two pod connection cables (174-3548-00). Order P3410 or P3420 pod separately.
Opt. 1R – Rackmount. Floppy drive moved to front panel.

Recommended Accessories
P3410
TTL level Pod with 12 Output Channels.
Includes: Pin Header-to-Pin Header Output Cable Set (012-1502-00) for 12 output channels, ISO Qualified Inspection Passed Certificate.
P3420
Variable level Pod with 12 Output Channels.
Includes: SMB-to-Pin Header Output Cable Set (012-1504-00) for 12 output channels, ISO Qualified Inspection Passed Certificate.

DG2000 Series
Power Plug Options

DG2000 Series Service
Opt. D3 – Calibration Data Report 3 Years (with Option C3).

P3410 and P3420 POD Service

Recommended Accessories
PODS (DG2020A)
Cables, Adapters and Connectors
SMB-to-Pin Header Cable (20 in.) – Order 012-1503-00.
SMB-to-Pin Header Cable (50 in.) – Order 012-1506-00.
Pin Header-to-Pin Header Cable – Order 012-1505-00.
SMB-to-SMB Cable (40 in.) – Order 012-1548-00.
50 Ω BNC-to-BNC Cable (Single shield) – Order 012-1342-00.
50 Ω BNC-to-BNC Cable (Double shield) – Order 012-1256-00.
50 Ω BNC-to-SMB Cable (40 in.) – Order 012-1459-00.
50 Ω BNC Male to SMB Female Adapter – Order 015-0671-00.
One-channel Pin Lead Set (Set of 5) – Order 012-1508-00.
Four-channel Pin Lead Set (Set of 3) – Order 012-1509-00.
Connector (for Pin-header) – Order 131-5919-00.
GPIB Cable – Order 012-0991-00.
Replacement 1.2 m POD Connection Cable (standard accessory) – Order 174-3548-00.
50 Ω SMA male to SMA male; 12 in. – Order 174-1364-00.
50 Ω SMA male to SMA male; 20 in. – Order 174-1427-00.
50 Ω SMA male to SMA male; 60 in. – Order 174-1428-00.
50 Ω SMA male to SMA male; 2 m – Order 174-0679-00.
50 Ω SMA male to SMA male; 8.5 in. – Order 174-1120-00.
50 Ω SMA male to SMA male; 1 m – Order 174-1341-00.

Documentation

Warranty – One year parts and labor.