The xbusvga directory contains the Xilinx design, while the xbuc directory contains the Keil C project.

This uPC code is not optimized, so it runs well off the theoretical limit of 500k/sec. It runs about 12-15kbytes/sec currently.

The interface provided in xbus.c is as follows:

```c
XWrite(addr, data);
data = XRead(addr);
```

The streaming features of Xbus are not currently available through this interface. A couple of new procedures (like XwriteNext and XreadNext) would need to be implemented.

The Xilinx design contains a memory mapped register (address 0xffff) that is used to control the panning of the vga screen. The register shares this address with the sram, so that a write to address 0xffff affects both the register and sram.

This design did not work for us with a standard parallel cable. The status pins on the parallel cable needed to be electrically isolated from the PC. We did this by rewiring an old Xilinx Xact Dongle.