TUTORIAL #0:
INTRODUCTION TO CREATING AND SIMULATING SIMPLE SCHEMATICS

This tutorial will introduce the tools and techniques necessary to design a basic schematic. The goal of this tutorial is to familiarize you with Active-HDL and to help you complete your assignment. After finishing this tutorial you will know how to:

- Start Active-HDL.
- Create a new workspace and design
- Add and remove files to and from a design.
- Place parts in a schematic design from the built-in library.
- Use wires in a schematic design.
- Run a basic simulation.

Start Active-HDL

First, start Active-HDL by double-clicking the icon located on your desktop. If the icon is not present then select the Windows button on the left of the taskbar and select “All Programs > DEV TOOLS & LANGUAGES > Aldec > Active-HDL 8.2.”

Create a new workspace

A workspace holds your designs, and each design may consist of many files (i.e. schematics, Verilog source code, etc). When you open Active-HDL, you may be presented with the License Configuration window (Figure 1). Press ‘Next’ to advance to the next screen.

![License Configuration Window](image)

Figure 1

At this point you should see the Getting Started window (Figure 2), which allows you to create a new workspace, or open an existing workspace (once you have created other workspaces, they will appear in the field at the center of this window). The ‘More…’ button allows you to browse for existing workspaces.
1. Select the “Create new workspace” option and press the ‘OK’ button to open the New Workspace window (Figure 3):

2. Enter a **descriptive** name into the ‘Type the workspace name’ field.
3. Change the workspace directory by entering it in the ‘Select the location of the workspace folder’ field, or use the “Browse” button to select the new directory. We strongly recommend you use your student drive.

   **Note:** Files saved to the local drive will be automatically deleted on logout.

4. Select the ‘Add New Design to Workspace’ check box if it is not already checked.
5. Your New Workspace window should look similar to Figure 4. If so, click the OK button, and continue.

   **Note:** if you use the naming scheme shown in Figure 4, replace ‘###’ with the course number, and replace <quarter> and <year> with the quarter and year you are taking the course.
6. If you are creating a new workspace, as in the previous steps, you will see the Design Browser dialogue (Figure 5). Select ‘Yes’ to create the new design.

Create a design
After creating a workspace, the New Design Wizard (Figure 6) walks you through creating a design. A design can consist of one or more Verilog modules, schematics, and other design files. A workspace, as mentioned earlier, can contain one or more designs. You can add more designs later by selecting File > New > Design in the menu bar. For now, we will add the first design to the workspace by following the steps provided on the following pages.

1. Click the ‘Create an Empty Design with Design Flow’ radio button as shown in Figure 6. Then click the ‘Next’ button.
2. Find the ‘Block Diagram Configuration’ field and select the “Default HDL Language” option. Make sure the ‘Default HDL Language’ field is set to “VERILOG.” Leave the default settings in the ‘Flow Settings’ portion of the window since we will not be synthesizing yet. Your New Design Wizard window should look like Figure 7. If so, then click the Next button.
3. In the ‘Type the design name’ field, type a name for your new design. The name must contain only letters, numbers, and underscores (“_”), and cannot start with a number (i.e. 4bitadder is invalid, however four_bit_adder is valid). Use descriptive names that do not match file names, other design names, or workspace names. By default, the design directory is under the workspace directory, and the name of the default working library of the design is the same as the design name. Leave these default values alone.

**Warning: the directory path should not contain any spaces in it.**

Your window should look like Figure 8, although you can use a more descriptive name than “lab_1”.

4. Double check your file name and location, and then click the ‘Next’ button.
5. Make sure that your design name and design directory are both correct in the window that follows (Figure 9). If not, click the ‘Back’ button to make any changes, or click the ‘Finish’ button to create the design.
Add a Block Diagram (schematic) file
At this point your screen should look like Figure 10. The frame on the left is called the Design Browser and lists all of the components in your design. The frame on the bottom is the Console and is where status and error messages are printed. If these frames are not open, or if you have closed them by accident, you can open them by going to View in the menu bar. In the center of the screen is the main window where you will draw your schematics. When your design is first opened, the Design Flow Manager opens in this window. We won’t be using this tool during this tutorial. At the top of this window is the Standard toolbar. Finally, notice the tab at the bottom left side of the main window. As you create schematics and other components in your design, you can use the tabs at the bottom of this window to make the corresponding file active in the main window.
6. Double-click the ‘Add New File’ option in the *Design Browser* (Figure 11). This will open the *Add New File* window.
7. Click the ‘Empty Files’ tab in the Add New File window. Select the ‘Block Diagram’ icon, type a descriptive name into the ‘Name’ field, and then click the ‘OK’ button (Figure 12).

8. Notice that the schematic file has been added to the design in the Design Browser on the left. Schematic files in Active-HDL are called Block Diagram files and have an extension of “.bde”. The question mark means the file has not been compiled yet, which we will get to later. Also, new toolbars have been added below the standard tool bar (which are used to edit block diagrams) and the block diagram has been opened in the main portion of the window, with a new tab along the bottom (Figure 13).
Place parts into your schematic design
Now you are ready to build your gate logic. The steps below will teach you how to add basic gates to your schematic and how to add single bit input and output terminals. Additionally, you will need to know how to move and delete gates to clean up your design’s appearance.

Note: this tutorial uses the icons in the toolbars and other shortcuts to access most of the tools in Active-HDL; however, all the commands accessed from the toolbars can be found in the menu as well.

Figure 14 is the final version of the schematic you will be drawing. Your final design should look similar with two inputs (A & B), two gates (AND & OR), and two outputs (Y & Z).
1. **Do not use the ‘Built-in’ symbols.** Instead, you are required to use the components located in the standard class library called “lib370”. To add the symbols for the components in the standard class library to the symbols toolbox, use the *Library Manager*, which you can open by clicking the ‘Library Manager’ icon in the toolbar (Figure 15).

2. Locate the lib370 library in the left frame of the main window, **right-click** it, and select the ‘Add to Symbols Toolbox’ option from the context menu (Figure 16).
3. Close the Library Manager by clicking its icon in the toolbar, right-click on the ‘libraries’ tab at the bottom of the main window and select ‘Close,’ or select File > Close from the menu bar at the top.

4. You will now add the 2-input AND gate and 2-input OR gate to your schematic to match the ones shown in Figure 14. Open the Symbols Toolbox by clicking the ‘Symbols Toolbox’ icon in the toolbar (Figure 17).

5. Click the plus symbol to the left of the “lib370” option to expand the list (Figure 18). Scroll down the to find the desired part from the list, or type in the name of the part in the field at the top of the Symbols Toolbox to search the list.
6. Click on the parts name in the list and notice that its symbol appears at the bottom of the Symbols Toolbox (Figure 19).
7. Add the part to your schematic by dragging the symbol from the Symbols Toolbox into your design (Figure 20). Continue until you have added all of the pink parts seen in Figure 14.
8. Active-HDL uses the standard Windows user-interface to select, move, and copy items in the schematic (i.e. drag, Ctrl-drag for copying multiple parts, Ctrl-z for undo, etc.). Figure 21 is an example of Ctrl-drag.
9. To add a terminal, click the drop down arrow next to the ‘Terminal’ icon in the toolbar (or select Diagram > Terminal in the menu bar). Click the appropriate terminal option in the drop-down menu (Figure 14 has two input and two output terminals).

![Figure 22](image)

10. Click in the schematic where you want to place the terminal.
11. Notice that you can continue to click and add multiple terminals (Figure 23 shows a user in the process of adding a second input terminal to the schematic). To stop adding terminals, press the Esc key.

![Figure 23](image)

**Note:** The Esc key is very useful to “get out” of just about any process (i.e. drawing wires, placing components, etc).

12. There are many ways to rename a terminal from its default name. One way is to right-click on the terminal and select ‘Properties’ from the context menu. This will display the *Terminal Properties* dialogue (as shown in Figure 24). Rename the terminal by typing the desired name in the ‘Name’ field.
Moving gates and terminals is as easy as clicking and dragging the part to the new location. Additionally, the arrow keys are very useful for moving components precisely where you need them in the schematic. To delete parts, simply click the part to be deleted (when properly selected, the part will be outlined in a red box), and then press the Delete key.

**Using wires in Active-HDL**  
At this point you should have the gates and terminals added to your diagram to match those in Figure 14. This part of the tutorial will show you how to make connections using wires, how to move the wires, how to name wires, and how to delete wires.

1. Click on the Wire icon in the toolbar (see Figure 25).

2. Now click anywhere in the schematic and drag your mouse to the point in the schematic where you want the wire to end. Clicking on a port or terminal will connect an end of the wire to that port or terminal, clicking on another wire will create a junction, clicking on an empty space in the schematic will create an anchor or bend in the wire at that point, and double-clicking an empty space in the schematic will create an end to the wire at that point.
3. When you are done placing wires, go back to select mode by pressing the Esc key or clicking the ‘Select Mode’ button in the toolbar.

Removing wires:
4. Select the wire by clicking on it (the selected wire will turn red).

![Diagram of selected wires](image)

Figure 26

5. Press the Delete key.

Note: while you may draw a wire with one or more bends in it in one motion, selecting a bent wire will only select the straight section under the cursor.

Moving wires:
6. Click and drag on the wire or part of the wire to be moved.
7. Drag your mouse to the new location and release the button.

Checking, saving, and compiling your design
At this point you should have a schematic with gates and terminals connected using wires (and it should look similar to Figure 14). However, your file in the Design Browser is still preceded by a question mark. Before you can run simulations you need to compile your design, at which point the question mark will become a green check mark if all is well, or a red “x” if there are errors.

1. Always save your files first. To do this, click the Save icon in the toolbar, or press Ctrl-S with the file’s tab active in the main window. Remember to save early and often throughout the design process.
2. Active-HDL provides a “Check Diagram” tool. This tool will verify that the components are connected properly by printing the results into the Design Rule Check report (DRC). Always use the “Check Diagram” tool prior to compiling by clicking the Diagram > Check Diagram option in the menu bar (see Figure 27).
3. When you run the check diagram tool, a DRC report file is created. Open this file by going to the DRC line in the Console and double-click the appropriate line (see 20). This file will list any errors or warnings your design might contain, such as unconnected ports, mislabeled wires and/or terminals, and other connection related errors/warnings. Each error/warning in the report is a hyperlink that will take you to the problematic component in your design. Figure 28 shows an example of a DRC report file for a schematic with a warning.
4. After you have checked your diagram and resolved any errors or warnings, click the ‘Compile’ icon in the Standard toolbar (see Figure 21). The Console window will display the results of the compilation. When compiling a schematic, the console will generally compile successfully even if there are gates and/or terminals that are not connected (in some cases, warnings will be issued for unconnected ports). Therefore, just because a schematic compiles does not mean that it will do what you intended it to do during simulations. This is the reason you need to check your diagram prior to compiling. Figure 29 shows a successful compilation.
Simulating a design
To ensure that your design functions as you intend, you need to simulate it. This portion of the tutorial will show you how to set the top-level, how to open a waveform, how to add signals to a waveform, and how to use “stimulators”.

Important: close all open waveforms from previous simulations, if any, prior to running a new simulation.

1. Before you can simulate a design, you must set the top-level. Since designs can be composed of multiple files or layers, we need to tell Active-HDL which file is our top level. After you compiled your block diagram file, two files were created: a Verilog file, and a module. Expand your block diagram file list by clicking the plus symbol next to the file name in the Design Browser. Continue to expand the list until you see the module, which is proceeded by an “M” icon (as seen in Figure 30).
Note: the following design entities are valid choices when setting the top-level: a configuration [“C” icon], a module [“M” icon], or an EDIF cell [“D” icon].

2. Right click the module and select the “Set as Top-Level” option. If you do not set the top-level, Active-HDL will “ask” you to do so when you attempt to initialize a simulation.

3. Select ‘Initialize Simulation’ under Simulation in the menu bar (Figure 32).
After selecting ‘Initialize Simulation’, notice in Figure 33 that the ‘Structures’ tab is opened in the *Design Browser*. 
4. Click the ‘New Waveform’ icon in the Standard toolbar.

5. Click the file name in the top window in the Design Browser under the ‘Structures’ tab. Notice in Figure 35 how the signals and wires (Nets) appear in the bottom window of the Design Browser.
6. Add the signals to the waveform by dragging the signals one by one into the left side of the waveform. A faster method of adding signals to the waveform is to select the signals using the Shift or Ctrl keys. Now you may drag them as described above into the waveform. You can also right-click on a selected signal, and click the Add to waveform option in the context menu as shown in Figure 36. Adding one or more signals will open the Waveform window in the main portion of the screen.
7. To simulate a design, we have to provide values for the input signals. Active-HDL provides ‘Stimulators’ to drive input signals in a waveform. In the left half of the Waveform window, right-click on the input signal you wish to stimulate and select ‘Stimulators…’ from the context menu as shown in Figure 37.
8. The *Stimulators* window will pop up with the ‘Signals’ tab active. The large arrow points to a list of stimulators, and your signal is shown on the left side of the window in the signals field. The ‘Type’ list shows the different stimulator options: choose the ‘Clock’ option. See “Using Stimulators” at the end of this tutorial to learn about some of the other options.
9. With the Stimulators window still opened, you can set additional signals by clicking the signals in the left side of the waveform. Once you have added the two input signals (i.e. A and B), choose a clock period of 10 ns for A by entering the time in second box from the left at the top of the window (see Figure 39). Click the Apply button.

10. Select a clock with a period of 20 ns for input B.

11. When you are finished applying your stimulators, click the Close button.

At this point, you are ready to run the simulation using the waveform and stimulators.
12. The “Run For” field located in the Standard toolbar controls how long to run the simulation. You may change this by using the up and down arrows to the right of the field, or you may type in a time.

![Image of the Standard toolbar with the Run For field highlighted](image)

Figure 40

13. You will use the default setting of 100ns for your simulation. Click the ‘Run For’ button in the Standard toolbar.

![Image of the Standard toolbar with the Run For button highlighted](image)

Figure 41

14. To restart the simulation, click the ‘Restart button’ in the Standard toolbar.

![Image of the Standard toolbar with the Restart button highlighted](image)

Figure 42

**Note**: if you make changes to the waveform by changing stimulators or adding/removing signals, you need to restart the simulation. Similarly, any change in the file means the file needs to be saved and recompiled prior to restarting the simulation. To end a simulation, simply click Simulation > End Simulation in the menu bar.

Figure 43 is an example of a simulation using the steps provided in this tutorial.

![Image of a waveform with signal names and values](image)

Figure 43

Now that you have run a simulation and created a waveform, you should save that waveform. With the Waveform tab active, press Ctrl-s to save, or right-click the tab and select save. Remember to use descriptive names. A good naming convention is <design name>_.wv. You may have several waveforms for the same design. This is very useful in comparing different signal values and methods of driving the input signals. However, you should **close all waveforms** when you are done to avoid confusing signals when simulating other designs. You
should experiment with the different methods available and save the results in separate waveforms for comparison; however, this is optional.

**Concluding Remarks**
This completes the first tutorial for Active-HDL there will be three other tutorials. Remember that this tutorial has only scratched the surface of the capabilities of this program. We strongly recommend you practice using the techniques described within this tutorial while experimenting with and exploring other methods and techniques that Active-HDL offers. Don’t be discouraged if you do not understand what all of the tools are used for or the concepts the tutorial covers that have not yet been covered in class. By spending time with this tool and experimenting, you will save time by being better prepared for the more complicated upcoming assignments.