Using Synplicity within Active-HDL

The Makefile supplied with the ML300 tools sets up everything to compile our platform to the Virtex 2 Pro. It is possible, however, to do this all in Active-HDL. While we won’t be setting this up, it can be very beneficial to run Synplicity on our designs in Active-HDL. Doing this will help us make sure we are designing circuits that will synthesize properly. It also avoids the overhead of synthesizing our entire design when we are only working with a single module or small set of modules. The following steps show how to setup Synplicity, analyze a single module, and synthesize an entire design tree, all within Active-HDL.

- Make sure the synthesis tools are setup for your design in Active-HDL:
  - On the menu bar, click “Design” and choose “Flow Settings…”
  - For “Tool name:” under **HDL synthesis**, choose “Synplicity Synplify Pro 7.x”
  - Make sure “Location:” is set to the location of synplify_pro.exe, which is “C:synplicity\Synplify_73\bin” on most machines
  - At the bottom of the box under **Defaults**, set “Family:” to “VIRTTEX2P”
  - It should not be necessary to modify any of the other settings

- To analyze a Verilog module using Synplicity, click on the “Analyze” button or choose Analyze from the Design menu.
In order to Analyze a design this way, the design must be written in Verilog (no schematics) and the code should not call any other modules. If other modules are called, the analysis tools will insert a “black box” in its place and several errors and warnings will be displayed.

- It is also possible to synthesize an entire design tree using the Design Flow Manager.
  - If the Design Flow Manager is not visible, click on the “View Flow” button or press Alt+3
  - Configure the synthesis options by clicking on “options” to the left of the synthesis block.
  - In the “Synthesis Options” box, exclude the files you do not want to synthesize by right-clicking them and unchecking “Include to synthesis.” Some files you will not want to include are test fixtures and test designs.
Choose a Top-Level Unit (the module at the top of the hierarchy) and the correct Family (VIRTEX2P). Modifications to other constraints such as “speed” and the constraints in the “Setting” tab are optional.

Click “OK” and then click on the synthesize block in the flow manager. Synplicity will start and you can click “Run” to synthesize the design.