# CSE352 Spring 2015 Homework #3

Instructor: Joshua Smith
TA: Hanchuan Li

Due Online on Catalyst: 4/24/2015

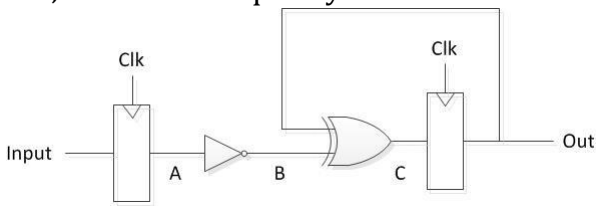
Homework will be graded on both effort and correctness. If you find yourself having trouble with a problem, write down what you know and how far you were able to get in order get partial credit. Solutions that are correct but do not adequately explain the question may not receive full credit. Solutions that are incorrect and show no work will not receive any credit.

You are encouraged to collaborate with your peers. However, each person must write up his or her homework assignments individually. Justice will be enforced if you are caught cheating. If you need an extension, you are required to submit a Haiku explaining why you need an extension BEFORE the homework deadline. Late homework is subject to a late penalty of 20 percent per day.

If you have any questions, please email to 'staff cse352 15sp@cs.washington.edu'

## Problem 1 *Critical Path*

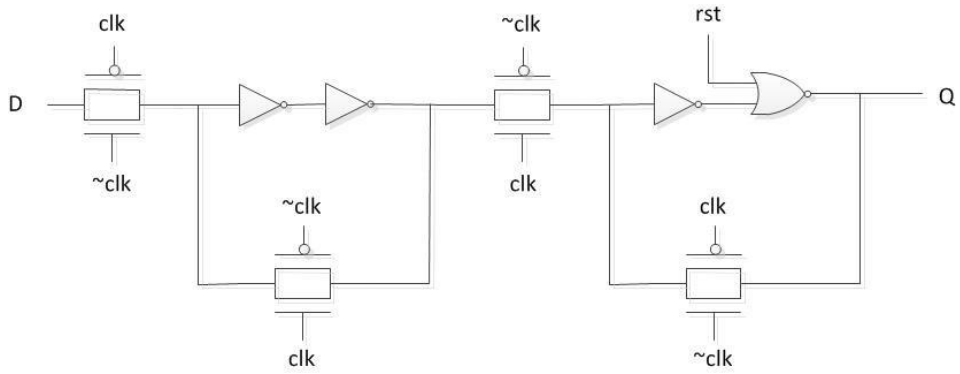
Consider the following circuit. The inverter has a combinational delay of 6ns and the XOR gate has a combination delay of 7ns. For the registers, assume the setup time is 0.5ns, hold time is 0.5ns, and clock-to-q delay is 4 ns.




What is the maximum possible operating frequency of this circuit?

## Problem 2 *Flip Flops*

Ben Bitdiddle and Sylvia Short-circuit are having an argument over how to implement an asynchronous reset to the following register using a signal rst. The asynchronous reset should immediately clear the value of the register and can be asserted for any period of time. He argues that the following modification is sufficient to implement the asynchronous reset:



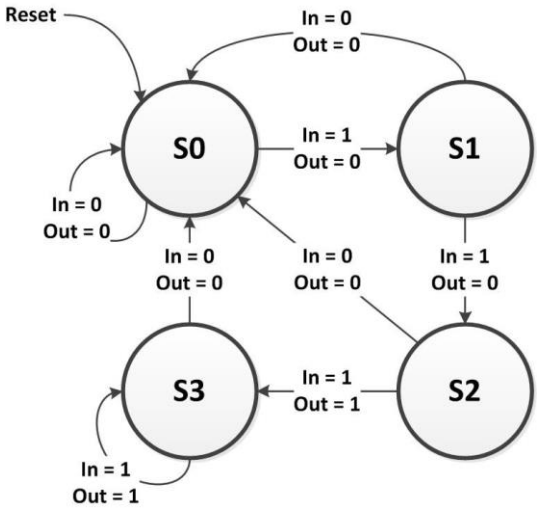

Sylvia Short-circuit disagrees and argues that Ben's solution does not actually work and that it will fail for certain cases. Who is correct? If Ben's solution is indeed incorrect, under what circumstances would his implementation fail and how would you fix it?

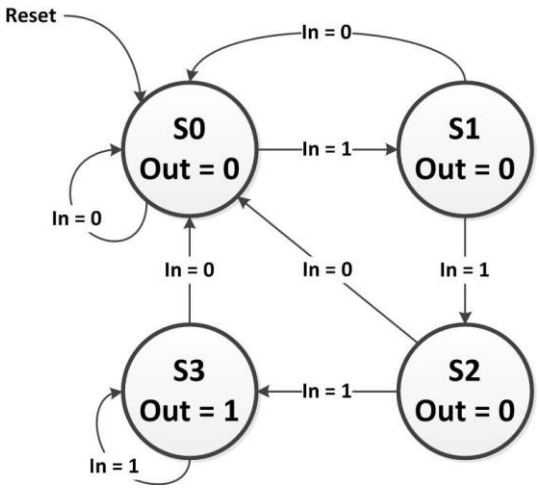
## **Problem 3** *Finite State Machines*

Consider the design of a simple edge detector circuit. The circuit has a one bit input In and a one bit output Out. Out should only be asserted for one cycle when the circuit detects a positive edge in the signal In (i.e. a transition from zero to one). The Out signal should be asserted the same cycle that the positive edge is detected (i.e. the cycle where the signal is high for the first time). Draw both the Moore and Mealy style FSM for this circuit. In addition, draw the corresponding circuit implementation for the Mealy style FSM using only registers and simple logic gates. (Make sure to include a reset signal Reset).

## **Problem 4** *Finite State Machines*

Ben Bitdiddle and Alyssa P. Hacker are arguing over whether the following two finite state machines are functionally equivalent. Ben argues that the circuits are functionally equivalent because they will both assert the signal Out after the input In is asserted for three consecutive cycles. Alyssa disagrees and argues that the FSMs are not functionally equivalent. Who is correct and why


Reset
In = 0
Out = 0
S0
In = 1
Out = 0
S1
In = 0
Out = 0
In = 0
Out = 0
In = 0
Out = 0
In = 1
Out = 0
S3
In = 1
Out = 1
S2
In = 1
Out = 1


Reset
In = 0
S0
Out = 0
In = 1
S1
Out = 0
In = 0
In = 0
In = 0
In = 1
S3
Out = 1
In = 1
S2
Out = 0