CSE352 Spring 2015 Homework #4

Instructor: Joshua Smith
TAs: Hanchuan Li, Boling Yang

Due Online Monday 5/4/2015

Please write your name and student ID at the top right corner of each page, and staple or paperclip your work together. We are NOT responsible for losing papers that were not stapled or paper clipped together.

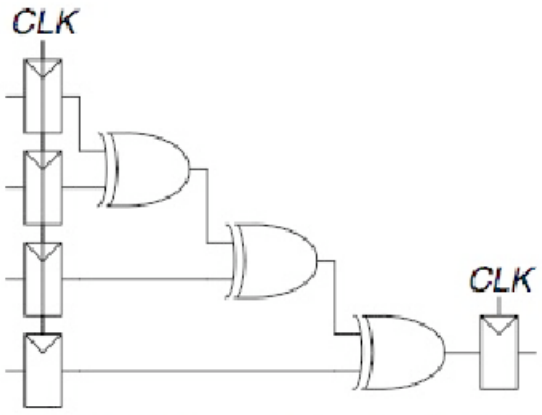
Complete the following questions. Please write legibly and try to draw clean diagrams. Spaghetti wiring in circuit diagrams is difficult to grade. We will not grade work that is too heavily encrypted for us to read (i.e. we can't read it, we can't grade it). Please consider typesetting your work if you think that it may not be legible to the grader. You are encouraged to collaborate with your peers but you must turn in your own work. Justice will be enforced if you are caught cheating.

Problem 1 *Finite State Machines*

Design a Mealy style FSM that takes a one bit input in and asserts a one bit signal out if the sequence 10010 has been detected. The out signal should be asserted the same cycle that the last 0 in the sequence is detected. Sequence can also overlap, for instance if the sequence 10010010 is input, the signal out should be asserted on the 5th cycle, and the 8th cycle. Minimize the number of states in your FSM. Make sure to also designate what the initial state of the machine will be on a reset.

Problem 2 *Carry Select Adders*

Ben Bitdiddle has designed the following circuit to compute a registered four-input XOR function. Each two-input XOR gate has a propagation delay of 100ps and a contamination delay of 55 ps. Each flip-flop has a setup time of 60 ps, a hold time of 20 ps, a clock-to-Q maximum delay of 70 ps, and a clock-to-Q minimum delay of 50 ps.



(a) If there is no clock skew, what is the maximum operating frequency of the circuit?

(b) How much clock skew can the circuit tolerate if it must operate at 2 GHz?

(c) How much clock skew can the circuit tolerate before it might experience a hold time violation?

(d) Alyssa P. Hacker points out that she can redesign the combinational logic between the registers to be faster and tolerate more clock skew. Her improved circuit also uses three two-input XORs, but they are arranged differently. What is her circuit? What is its maximum frequency if there is no clock skew? How much clock skew can the circuit tolerate before it might experience a hold time violation?

Problem 3 Blast from the Past (Review)

Draw the CMOS transistor implementation of the following Boolean expressions. Minimize the number of transistors used:

(a) $(A + BC)(DC + AEC)$

(b) $\overline{A}+\overline{B}\,\overline{C} + \overline{D}$