CSE352 Spring 2015 Homework #5

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Due Online Friday 5/15/2015

Please write your name and student ID at the top right corner of each page, and staple or paperclip your work together. We are NOT responsible for losing papers that were not stapled or paper clipped together.

Complete the following questions. Please write legibly and try to draw clean diagrams. Spaghetti wiring in circuit diagrams is difficult to grade. We will not grade work that is too heavily encrypted for us to read (i.e. we can't read it, we can't grade it). Please consider typesetting your work if you think that it may not be legible to the grader. You are encouraged to collaborate with your peers but you must turn in your own work. Justice will be enforced if you are caught cheating.

Problem 1   *Counter Design*

(a)   Design a 32-bit counter that adds 4 at each clock edge. The counter has reset and clock inputs. Upon reset, the counter output is all 0.
(b)   Modify the counter from part (a) such that the counter will either increment by 4 or load a new 32-bit value, D, on each clock edge, depending on a control signal, PCSrc. When PCSrc =1, the counter loads the new value D.

Problem 2   *Ripple-Carry and Carry-Lookahead Adder Delay*

What is the delay for the following types of 64-bit adders? Assume that each two-input gate delay is 100 ps and that a full adder delay is 320 ps.

   (a) A ripple-carry adder
   (b) A carry-lookahead adder with 4-bit blocks

Problem 3   *Shifter*

Design a shifter that always shifts an 8-bit input left by 2 bits. The input and output are both 8 bits. Explain the design in words and sketch a schematic.

Problem 4   *XOR unit*

Use 4 full adders to build a 4 bit XOR module. For example, if the inputs to the XOR module are A = 0111 and B = 1100, the output S should be 1011. Explain the design in words and sketch a schematic.

1 bit full adder example: