CSE352 Spring 2015 Homework #6

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TA: Hanchuan Li, Boling Yang

Due Online in Catalyst Dropbox 5/27/2015

Homework will be graded on both effort and correctness. If you find yourself having trouble with a problem, write down what you know and how far you were able to get to get partial credit. Solutions that are correct but do not adequately explain the question may not receive full credit. Solutions that are incorrect and show no work will not receive any credit.

You are encouraged to collaborate with your peers. However, each person must write up their homework assignments individually. Justice will be enforced if you are caught cheating. If you need an extension, you are required to submit a Haiku explaining why you need an extension BEFORE the homework deadline. Late homework is subject to a late penalty of 20 percent per day.

If you have any questions, please email to 'staff_cse352 15sp@cs.washington.edu'

Question 1. *Comparator Design*

Design the following comparators for 32-bit numbers. Sketch the schematics.
(a) Not equal
(b) Greater than
(c) Less than or equal to

Question 2. *Non-Volatile Memory*

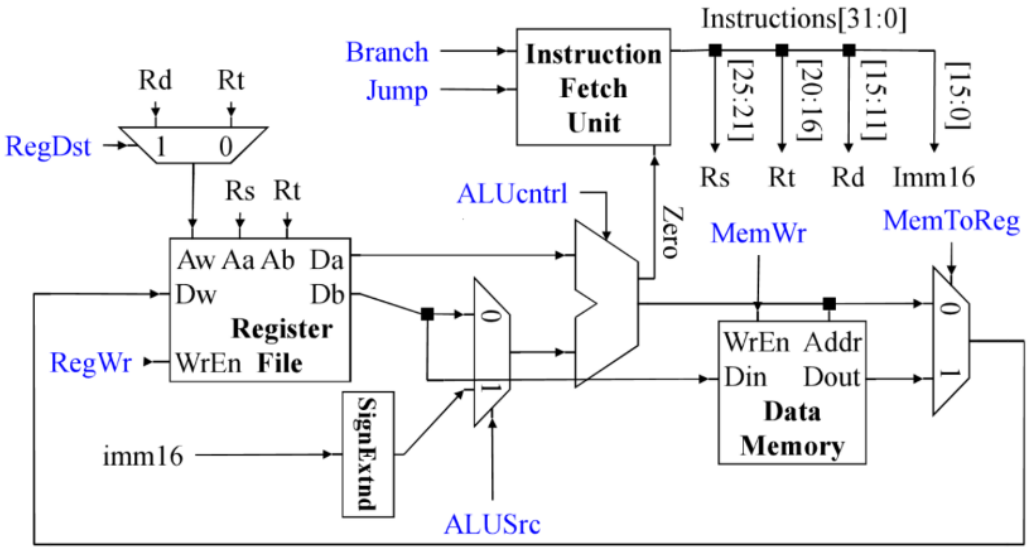
Many new forms of Non-Volatile Memory have been introduced in recent years, or are in development now. Choose a form of non-volatile memory, research it, and explain how it works. For example, you might choose from FeRAM, Phase Change Memory, "logic embedded" flash, ordinary flash, etc. Use a diagram illustrating a single bit of the memory. (If your memory has a floating gate, make sure to illustrate that, or whatever structure holds the state in a non-volatile fashion). Describe how a bit in the memory is programmed and erased. Properly cite your sources.

Question 3 *Single Cycle CPU*

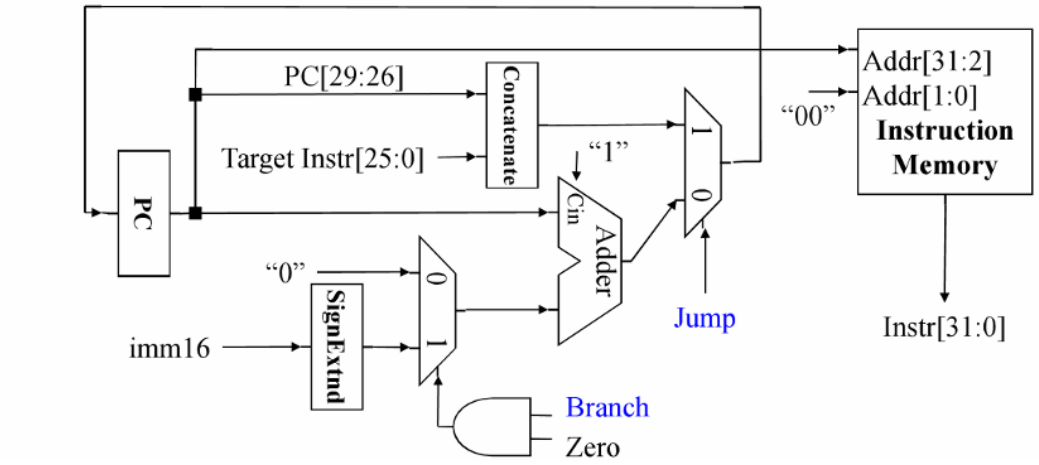
Take the single cycle processor below (next two pages) and indicate the data path and control logic for the following two instructions. You will draw on the 2 copies of this processor in order to indicate the data path for each instruction. If you need new hardware units and/or wires you may add them or change the existing units, but only as needed. Your machine must complete each of these instructions in a single clock cycle.

	sw	beq
RegDst		
AluSrc		
MemToReg		
RegWr		
MemWr		
Branch		
Jump		
AluCntrl		

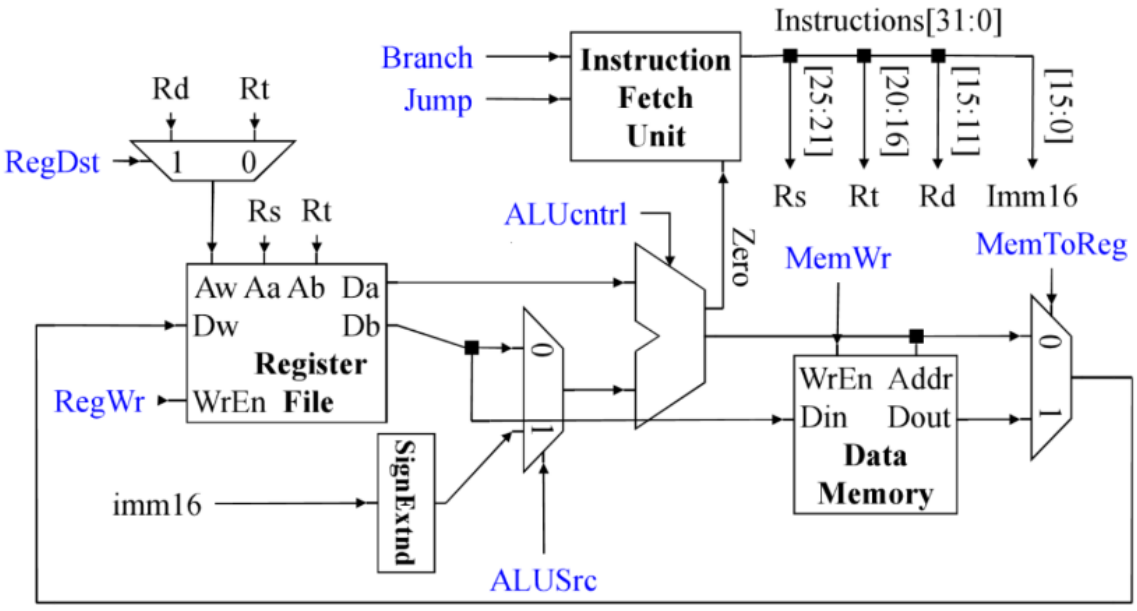
sw instruction



Instruction Fetch Unit:



beq instruction



Instruction Fetch Unit: