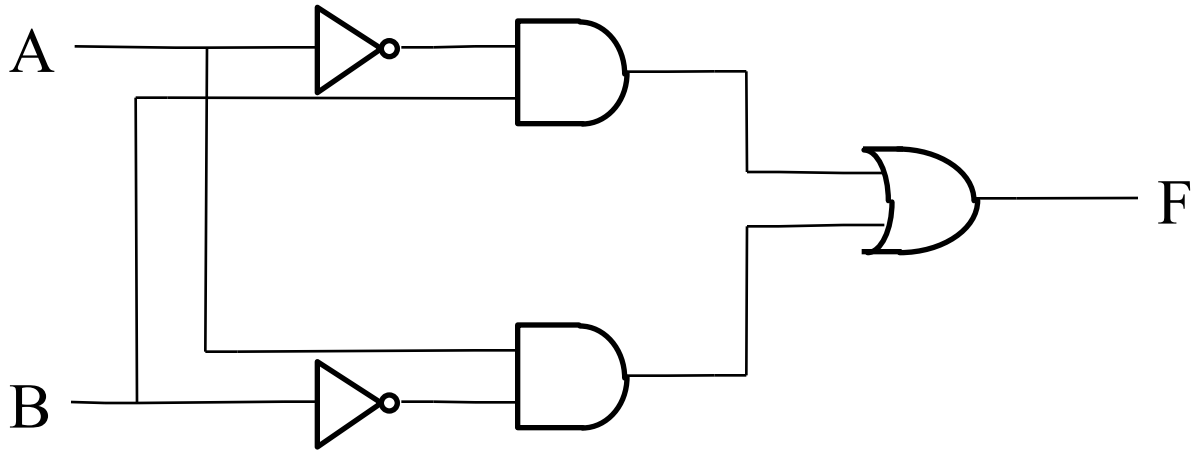
Review Problem 1

- Describe when the dome/interior light of the car should be on.
  - DriverDoorOpen = true if lefthand door open
  - PassDoorOpen = true if righthand door open
  - LightSwitch = true if light should be on regardless of door state, false if light should be on when a door is open

Review Problem 2

- What does the following circuit do?



Review Problem 3

- To buy beer, someone must be of age. Which of these sentences tells us exactly when Ann and Bob can get beer?
  1. It is not true that both Ann and Bob don't have ID.
  2. Ann has ID or Bob has ID or Both have ID.
  3. Ann has ID or Bob has ID
  4. Ann has ID and Bob does not, or Bob has ID and Ann does not.
  5. Ann has ID, or Bob has ID and Ann does not.

Review Problem 4

- Create the truth table for an equality circuit, which is true whenever the two inputs are the same.

Review Problem 5

- Write the Boolean equation for the 2nd seat belt light circuit on slide 7
  - Seat Belt Light (driver belt in, passenger belt in, passenger present):

Review Problem 6

- Does the following Boolean equation implement the function given in the truth table?

$$MyCout' = (A * B) + (A * Cin) + (A * B * Cin)$$

A	B	Cin	Cout
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

Review Problem 7

- Simplify the following Boolean Equation

$$AB + AC + \overline{\overline{A}}B$$

Review Problem 8

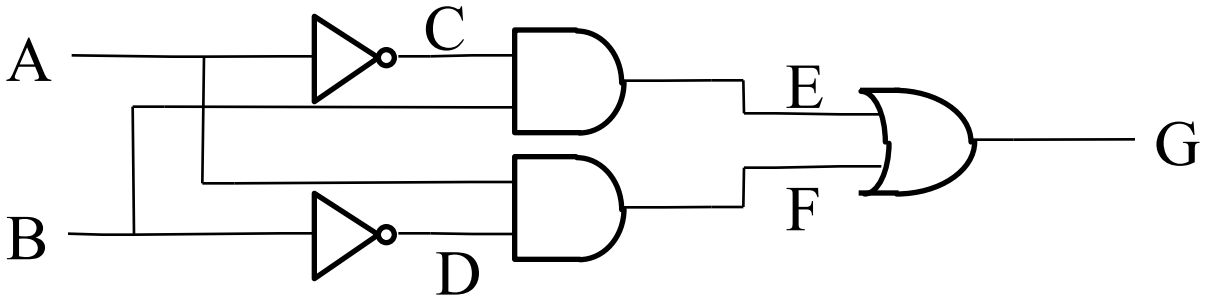
- Simplify the following Boolean Equation, starting with DeMorgan's Law

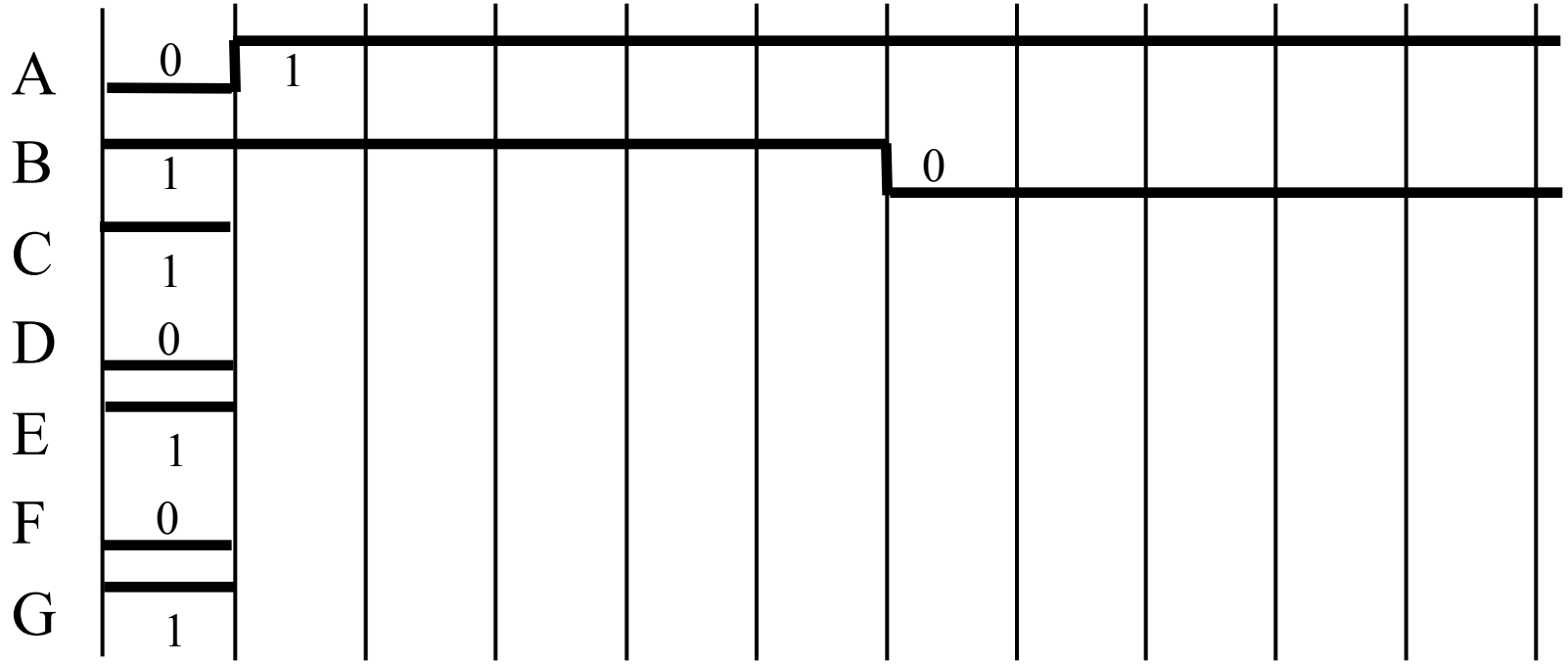
$$\overline{F} = A\overline{B} + AC$$

$$F =$$

Review Problem 9

- Assuming all gates have the same delay (including inverters), complete the following timing diagram.



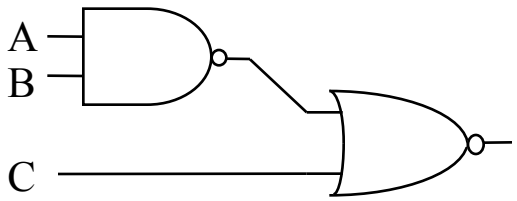


Review Problem 10

- Write the Verilog for a 2-input gate that is TRUE when an odd number of inputs are true.

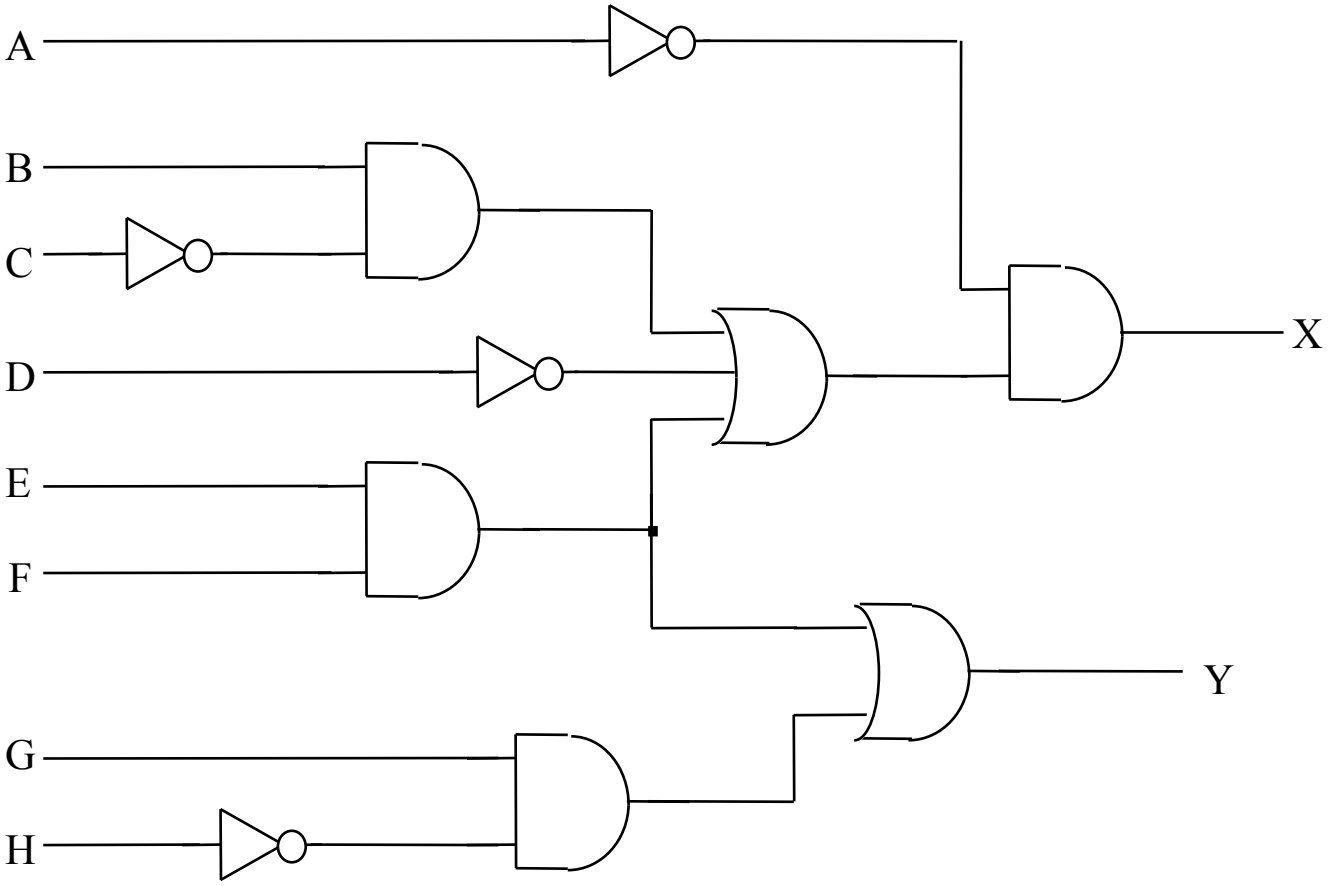
Review Problem 11

- What does this circuit do?



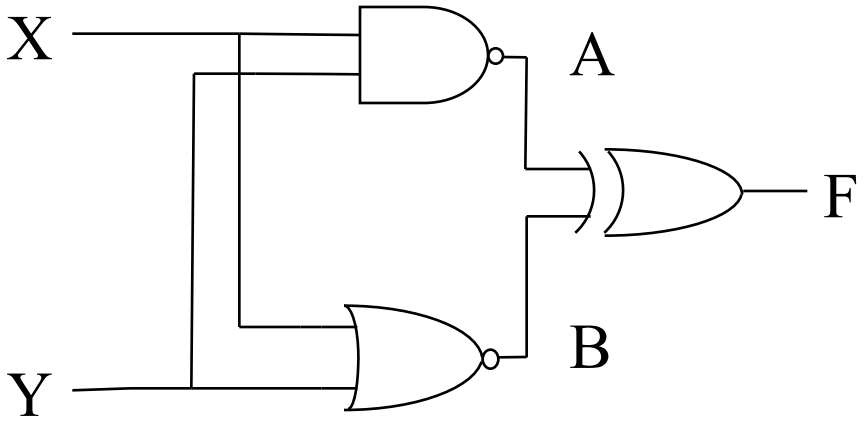
Review Problem 12

- Convert the following circuit to NAND/NOR form



Review Problem 13

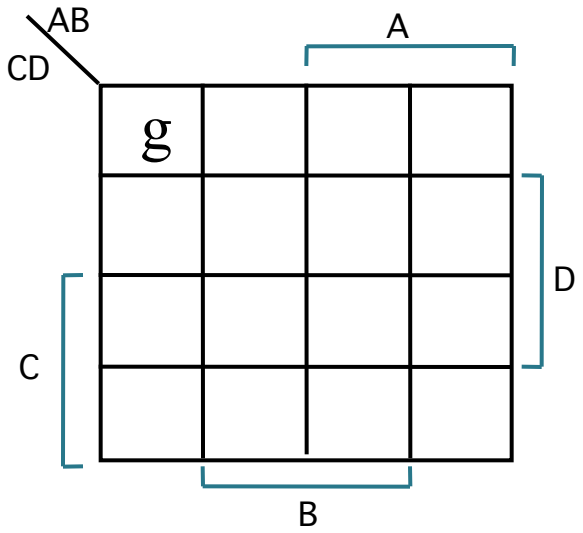
- What does this circuit do?



Review Problem 14

- Convert the Truth Table to a K-Map.
  - Letters are used as variables to hold the function value
  - First value already filled in.

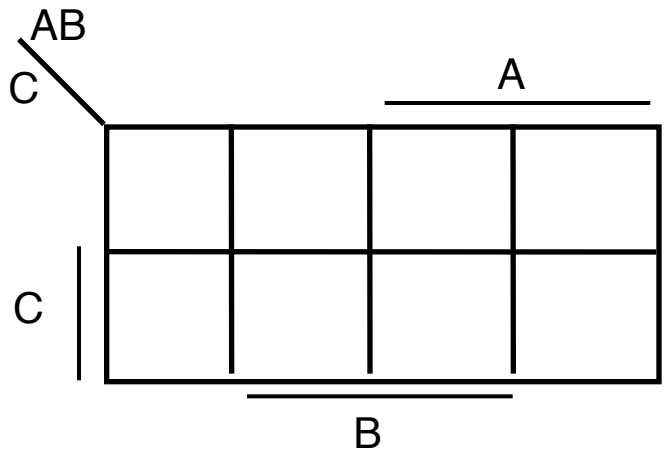
A	B	C	D	F
0	0	0	0	g
0	0	0	1	h
0	0	1	0	i
0	0	1	1	j
0	1	0	0	k
0	1	0	1	l
0	1	1	0	m
0	1	1	1	n
1	0	0	0	o
1	0	0	1	p
1	0	1	0	q
1	0	1	1	r
1	1	0	0	s
1	1	0	1	t
1	1	1	0	u
1	1	1	1	v



Review Problem 15

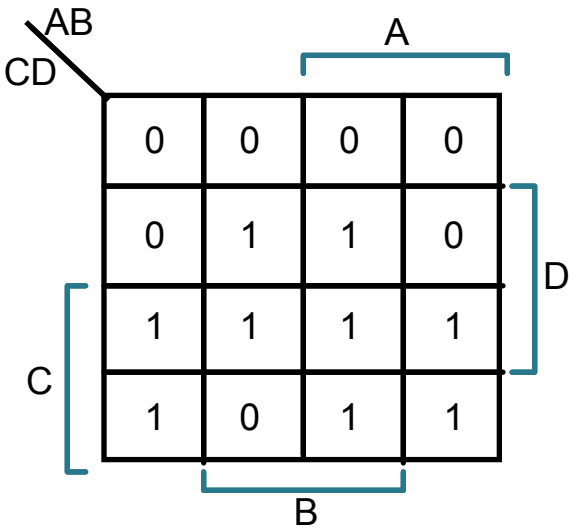
- Convert the Truth Table to a K-Map, then solve.

A	B	C	F
0	0	0	1
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0



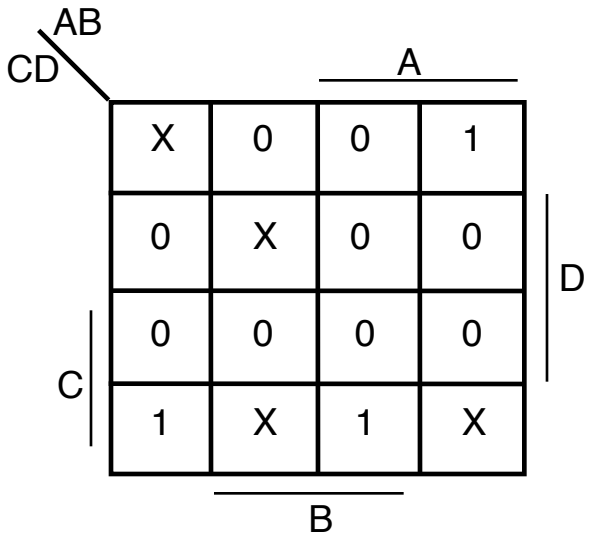
Review Problem 16

- Solve this K-Map.



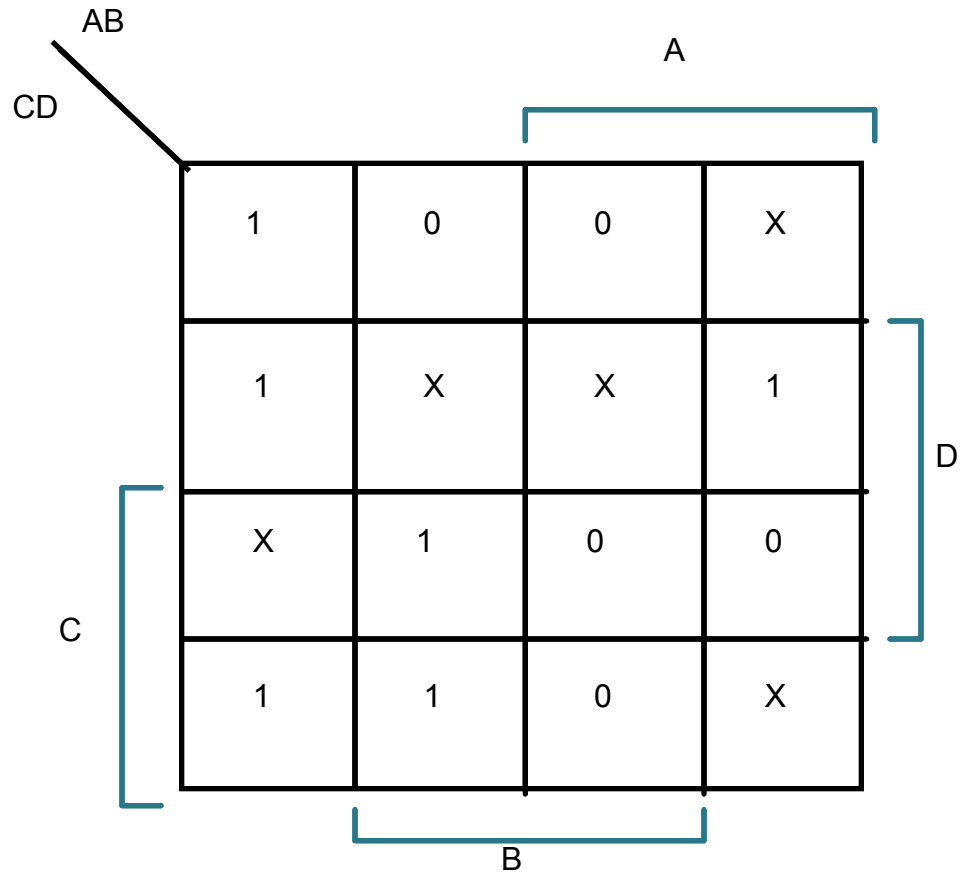
Review Problem 17

- Solve the following K-Map.



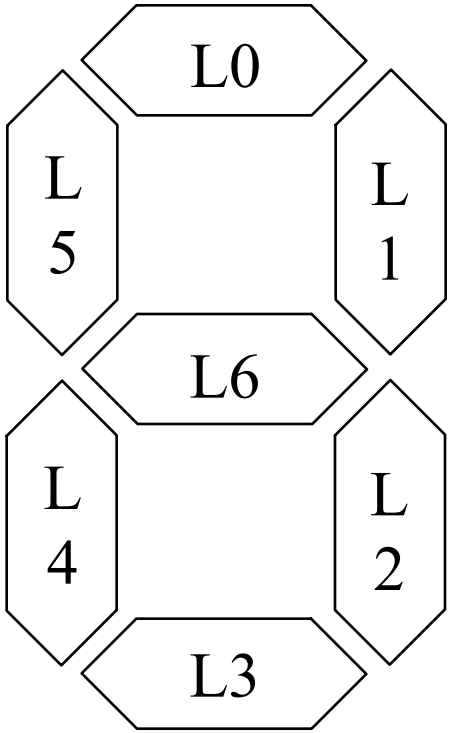
Review Problem 18

- Solve the following K-Map.



Review Problem 19

- Extend this Verilog code to also show the letter "A" on input pattern 1010 (ten) and "F" on pattern 1111 (fifteen).



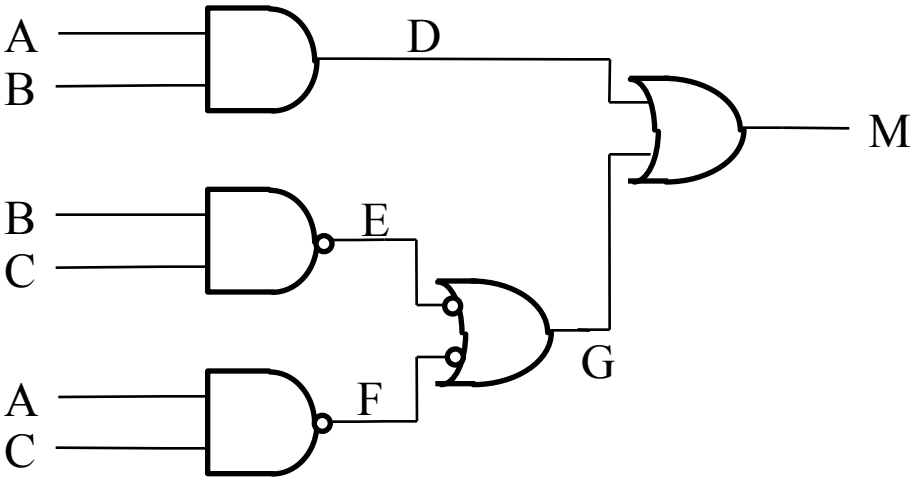

```
module seg7 (bcd, leds);
  input      [3:0] bcd;
  output reg [6:0] leds;

  always @(*)
    case (bcd)
      // BCD[]          LEDS[]
      // 3210           6543210
      4'b0000: leds = 7'b0111111;
      4'b0001: leds = 7'b0000110;
      4'b0010: leds = 7'b1011011;
      4'b0011: leds = 7'b1001111;
      4'b0100: leds = 7'b1100110;
      4'b0101: leds = 7'b1101101;
      4'b0110: leds = 7'b1111101;
      4'b0111: leds = 7'b0000111;
      4'b1000: leds = 7'b1111111;
      4'b1001: leds = 7'b1101111;
      default: leds = 7'bX;
    endcase
endmodule
```

Review Problem 20

- Amy, Bill, Carol, and Dennis each decide independently whether they want to play Chess or Checkers, each a 2-player game. Develop a circuit that can tell if the 4 people can be organized into two simultaneous games, respecting each person's choice.

Review Problem 21

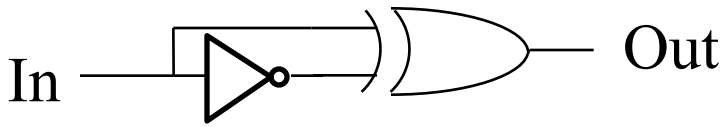
- For the buggy majority circuit below, the expected and the measured results are shown in the table. What gate is broken in this circuit?



Signal	Expected	Measured
A	0	0
B	1	1
C	1	1
D	0	0
E	0	1
F	1	1
G	1	0
M	1	0

Review Problem 22

- Can this circuit ever output a FALSE?



Review Problem 23

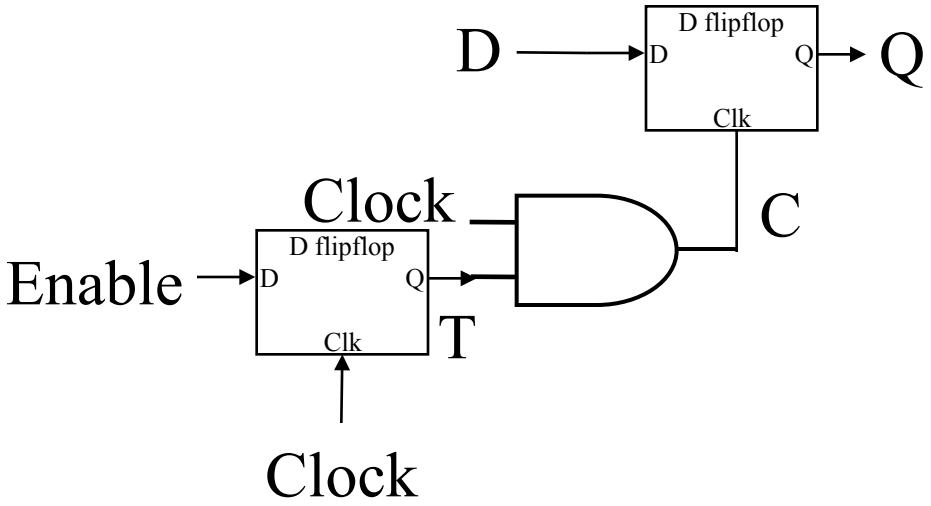
- The following two flip-flops are subtly different, but both useful. The difference in code is shown in bold. What is the difference in their behavior?

```
module D_FF1 (q, d, reset, clk);
  output q;
  input d, reset, clk;
  reg q;

  always @(posedge clk)
  if (reset)
    q <= 0;
  else
    q <= d;

endmodule
```

```
module D_FF2 (q, d, reset, clk);
  output q;
  input d, reset, clk;
  reg q;

  always @(posedge clk or posedge reset)
  if (reset)
    q <= 0;
  else
    q <= d;

endmodule
```

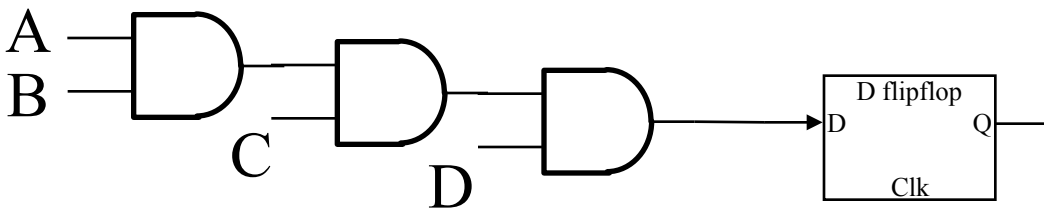
Review Problem 24

- In class we said we shouldn't put a logic gate on the clock input of a flipflop because of glitches. Does this fix the problem?



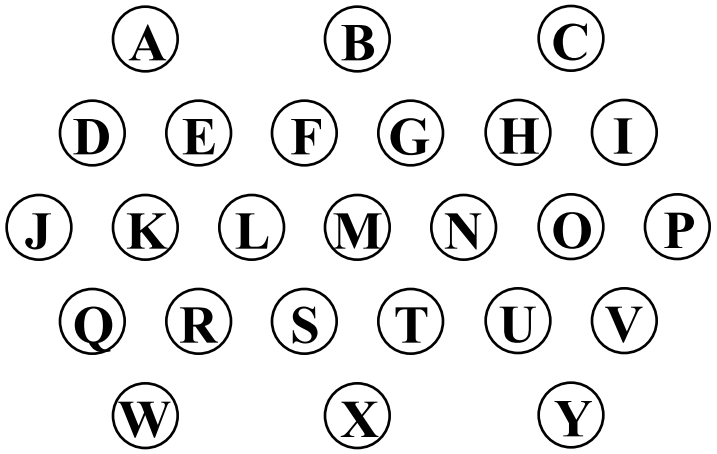
Review Problem 25

- If gate delays are 1.0ns each, T_{setup} is 0.5, and T_{hold} is 1.5, what is the best clock period for this computation?



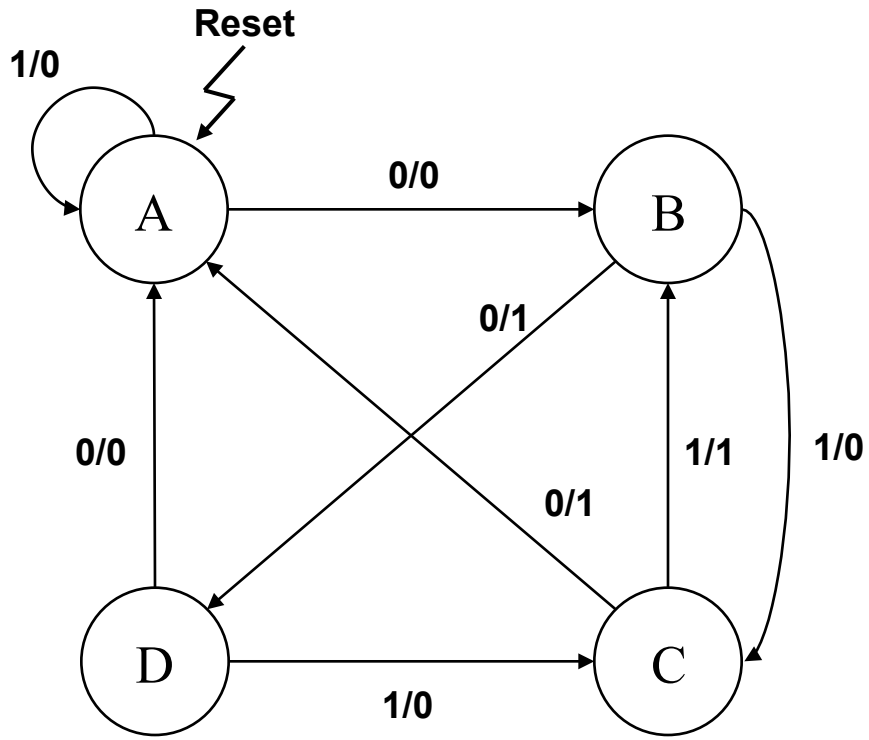
Review Problem 26

- Given the light display shown, build the FSM for a "move left" arrow traffic sign. It should animate an arrow moving left
  - Hint: Can any of the bulbs be connected to the same signal?



Review Problem 27

- What is the series of inputs that will produce the most TRUEs on the output



Review Problem 28

- An ambulance company wants a flashing yellow light that, when a button is held, will instead hold a solid red. Design this machine.

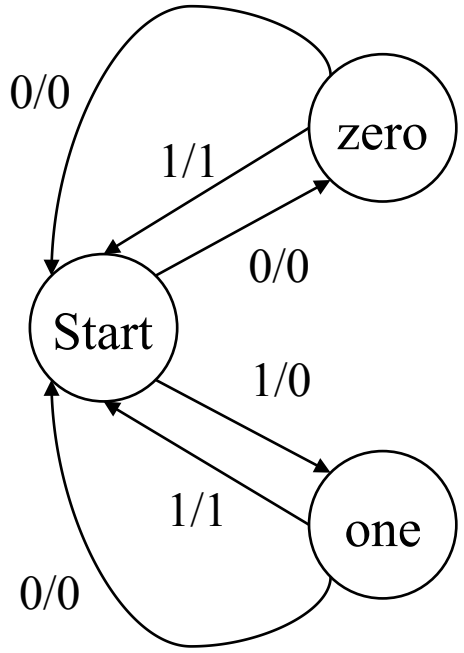
Review Problem 29

- Draw the circuit diagram for this code

```
module foo (clk, reset, in, out);
   input clk, reset, in;
   output reg out;
   parameter A = 1'b0, B = 1'b1;
   reg ps, ns;

   always @(*) begin
        case (ps)
        A: ns = B;
        B: if (in) ns = B;
           else ns = A;
        default: ns = 1'bX;
        endcase
        out = ps;
   end

   always @(posedge clk)
        if (reset)  ps <= 1'b0;
        else        ps <= ns;

endmodule
```

Review Problem 30

- What does this FSM do?



Review Problem 31

- Draw the state diagram of a machine that continuously outputs a true once at least two 0's and at least two 1's (in any order, not necessarily consecutively) have been seen, not including current input.

Review Problem 32

- Highway onramps have lights to meter cars entering the highway. Design the FSM for this, assuming we have a separate timer.

Review Problem 33

- Design a circuit to control the 7-segment display as an elevator floor indicator for a 4-story building.

Review Problem 34

- Which of the following numbers represents the largest value?
  - $(10011)_2$
  - $(23)_8$
  - $(13)_{16}$

Review Problem 35

- Convert the following value to binary
  - $(1000)_{10}$

Review Problem 36

- Perform the following conversions
- $(1101010010111101010)_2$ to hexadecimal

- $(4AF3)_{16}$ to binary

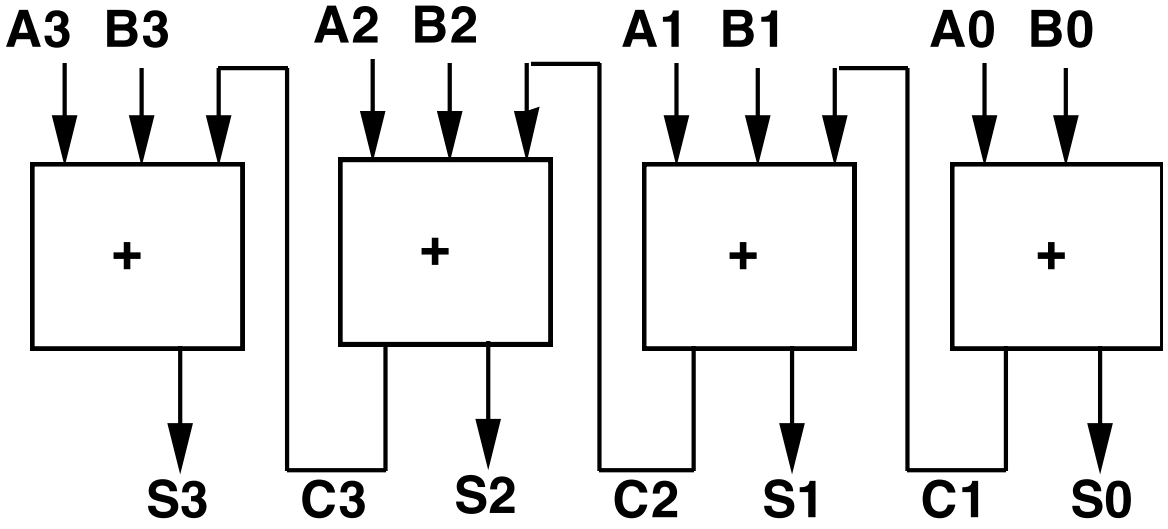
Review Problem 37

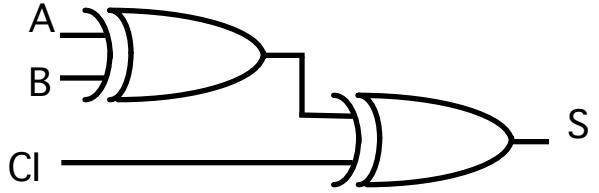
- Perform the following binary computations.

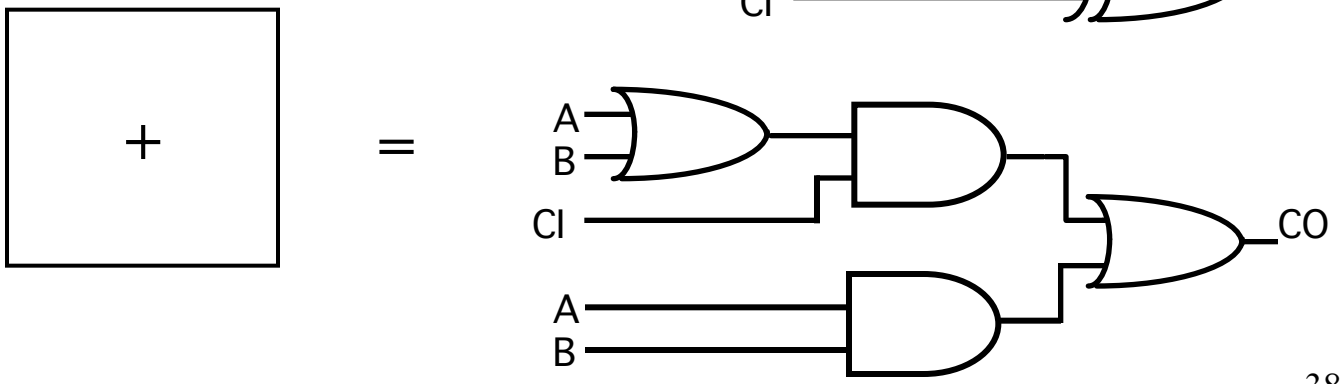
1 0 1 1 0	1 0 0 1	1 1 1
+ 0 0 1 1 1	- 0 0 1 1	* 0 1 1

Review Problem 38

- If all gates have a delay of 1ns, how long does a 4-bit adder take to compute?







Review Problem 39

- Create a **truth table** for a circuit which tells if a 3-bit number is evenly divisible by 3 (num/3 leaves no remainder). Have a separate output for the unsigned, 2's comp, and sign-magnitude versions.

B2 B1 B0	Uns	S-M	2's

Review Problem 40

- Perform the following computation in 2's Complement & Sign/Magnitude
  - Hint: convert subtraction to addition of the negation

2's Complement:

$$\begin{array}{r} 0\ 0\ 1\ 0 \\ -\ 0\ 0\ 1\ 1 \\ \hline \end{array}$$

Sign/Magnitude:

$$\begin{array}{r} 0\ 0\ 1\ 0 \\ -\ 0\ 0\ 1\ 1 \\ \hline \end{array}$$

Review Problem 41

- Convert the following numbers to decimal
- (1001) in 2's Complement:

- (1001) in Sign/Magnitude:

- (0101) in 2's Complement:

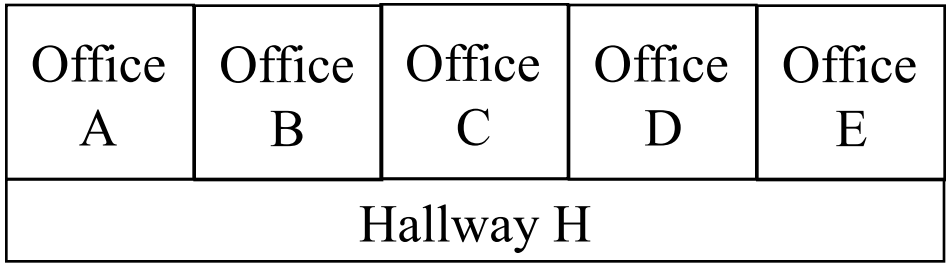
- (0101) in Sign/Magnitude:

Review Problem 42

- For the 6-bit 2's Complement number (111010)
  - How would it be represented in 10-bit 2's Complement?
  - What's the smallest number of bits required to represent that number in 2's Complement?

Review Problem 43

- An office building has an automatic lighting system based on motion sensors. An individual office light should be on if motion has been detected in the office within the last 5 minutes. Hallway lights should be on if any office lights on that hallway have been on, or any motion in the hallway detected, during the last 10 minutes. Design the system.



Review Problem 44

- If we only have inverters and standard 2-input gates, how many gates are needed to build a 3:8 decoder?

Review Problem 45

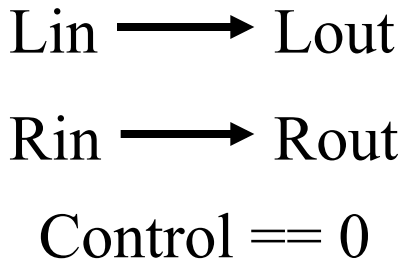
- Build a full adder using 3:8 Decoders and as few other gates as possible.

Review Problem 46

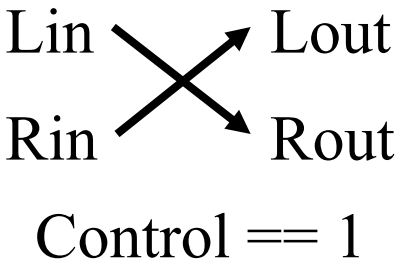
- Instead of a priority encoder, we plan to use the basic 4:2 encoder. However, we want an output "invalid" which is true when the encoder's assumption that only one input is true is not met. Design the circuit for this output.

Review Problem 47

- For a stereo, design a crossover box to deal with swapped speaker cables using **only muxes**.



Control == 0



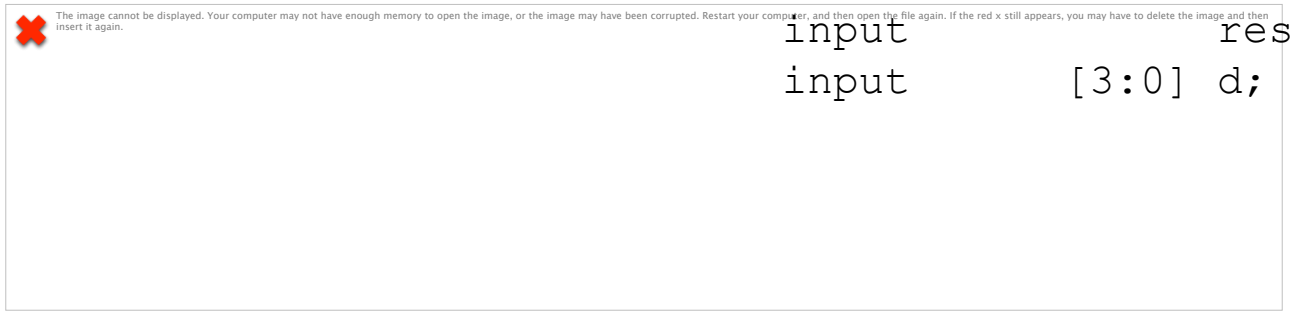
Control == 1

Review Problem 48

- Implement a 4:2 priority encoder using only 8:1 muxes and inverters

Review Problem 49

- Implement the controlled register from lecture in Verilog.




```
module reg4(out, reset, load, d, clk);
  output reg [3:0] out;
  input            reset, load, clk;
  input      [3:0] d;

endmodule
```

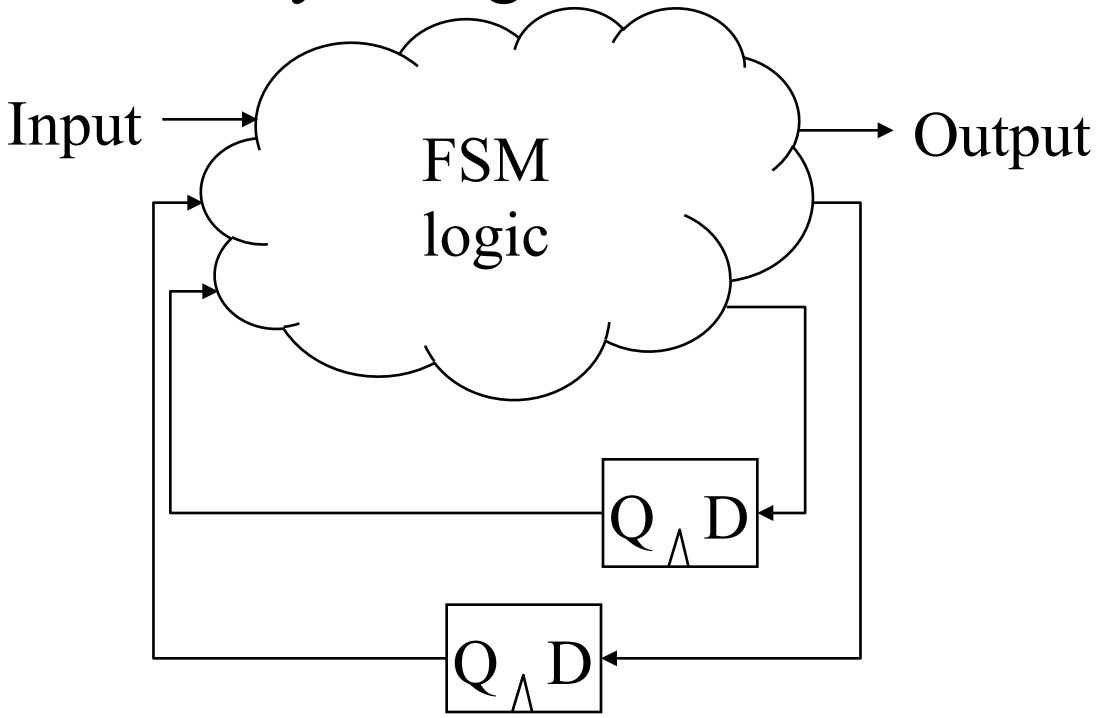
Review Problem 50

- Given what we know about about shift registers, what are the options for sending 32-bit values?

Wires	Cycles	Method

Review Problem 51

- I have already built an FSM to run at 5MHz, but I now need to use a 50MHz clock. How can I get it to still only change states 5M times a second?



Review Problem 52

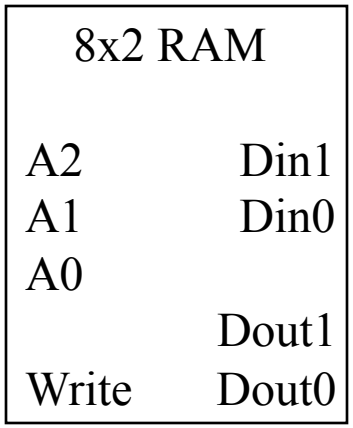
- Design a down counter that goes from 3 to 1 (then back to 3), with a parallel load.

Review Problem 53

- Build a 4x1 RAM. Use premade RAM cells, along with any standard components you need.

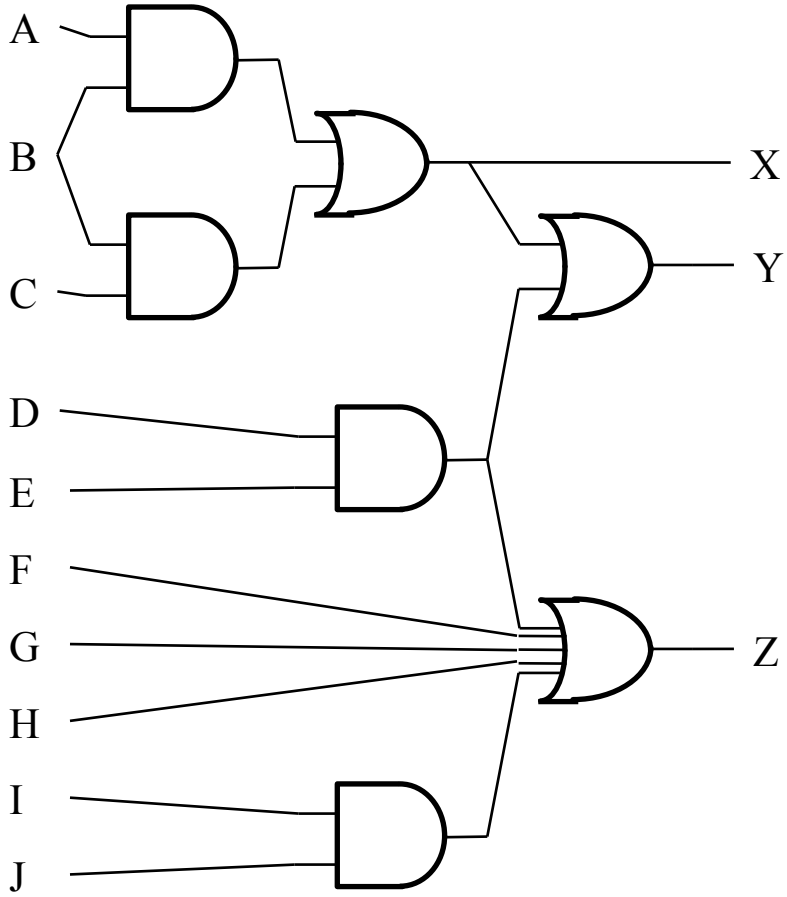
Review Problem 54

- If we only had 8x2 memories available, how could we make an 8x6 RAM?



Review Problem 55

- Implement this circuit with 4-LUTs



Review Problem 56

- What components are on your DE1-SoC board, and how are they connected?

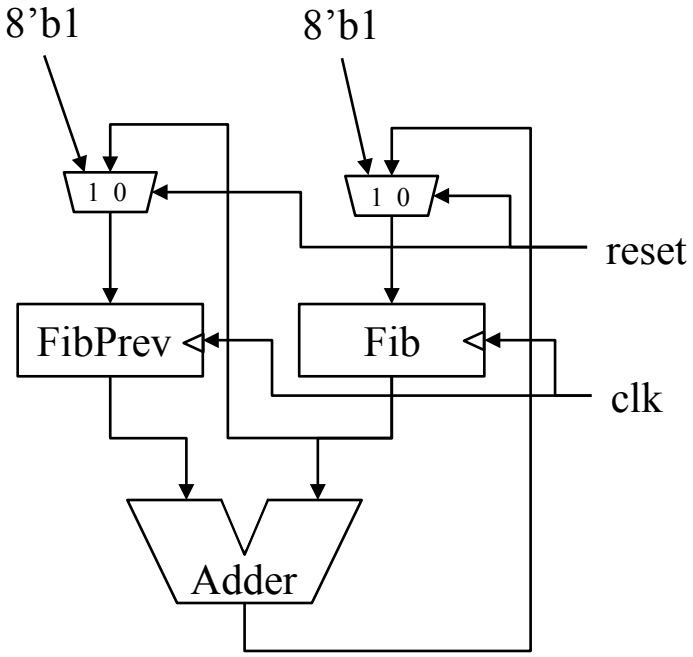
Review Problem 57

- Is the following good Verilog? If not, fix it. If so, draw the circuit it represents.

```
reg a, b, c;

always @(*) begin
   b = 0;
   c = 0;
   if (a)
      b = c;
   else
      c = b | d;
end
```

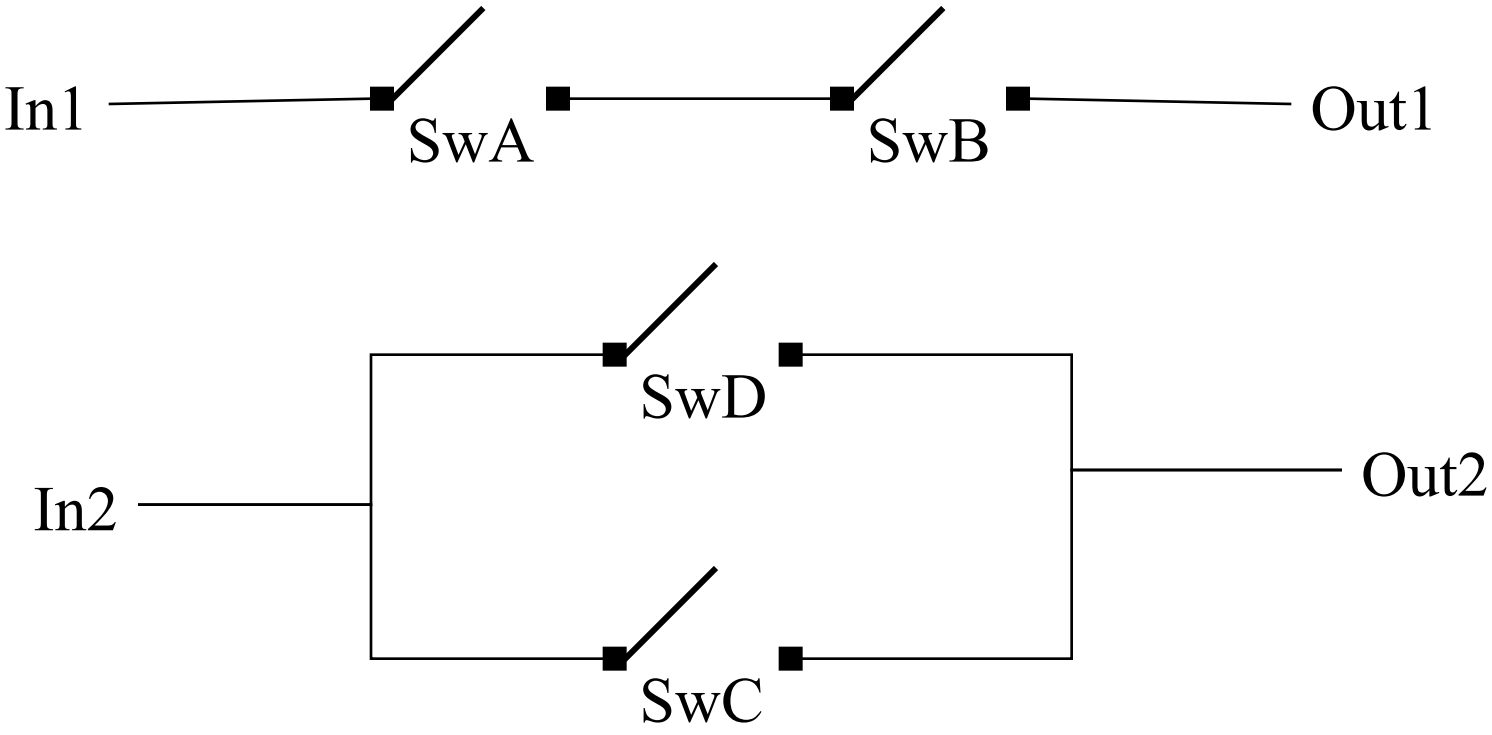
Review Problem 58

- Write Verilog that would create this circuit.



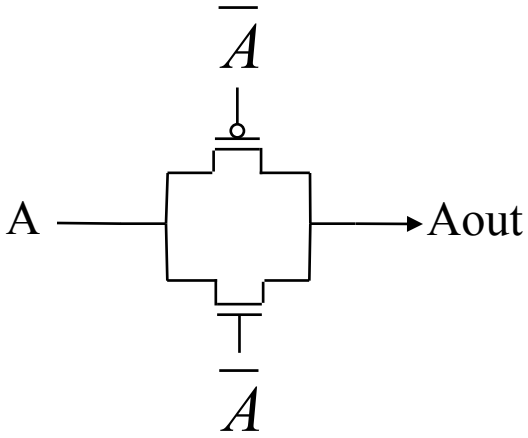
Review Problem 59

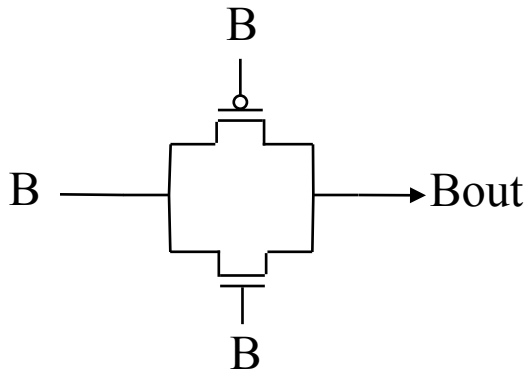
- When will current flow from the input to the output for each of these?



Review Problem 60

- What do these circuits do?





Review Problem 61

- Build an XOR gate from transistors. Assume you have two inputs, A and B, as well as their inverses ($\overline{A}$ and B).