University of Washington – Computer Science & Engineering

Spring 2019 Instructor: Justin Hsia 2019-04-30

CSE 369 QUIZ 1

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Please do not turn the page until 11:30.

Instructions

- This quiz contains 3 pages, including this cover page. You may use the backs of the pages for scratch work.
- Please clearly indicate (box, circle) your final answer.
- The quiz is closed book and closed notes.
- Please silence and put away all cell phones and other mobile or noise-making devices.
- Remove all hats, headphones, and watches.
- You have 20 minutes to complete this quiz.

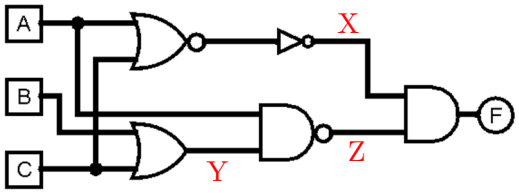
Advice

- Read questions carefully before starting. Read *all* questions first and start where you feel the most confident to maximize the use of your time.
- There may be partial credit for incomplete answers; please show your work.
- Relax. You are here to learn.

Question	Points	Score
(1) CL Gates	8	8
(2) K-map	5	5
(3) Waveforms & Verilog	11	11
Total:	**24**	**24**

Question 1: Combinational Logic Gates [8 pts]

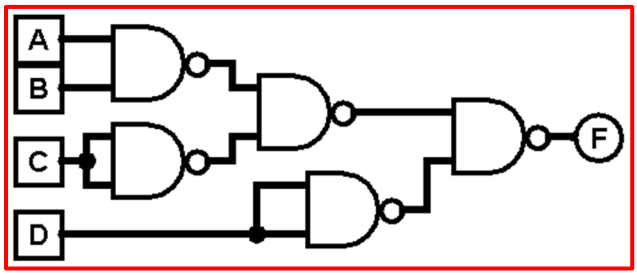
(A) Write out a Boolean expression for the circuit diagram below. *No need to simplify.* Remember to use + (OR), · (AND), and ¯ (NOT) as well as any necessary parentheses to make your answer unambiguous. [2 pts] $\mathbf{F = \overline{\overline{(A + C)} \cdot \overline{A(B + C)}}}$



X = $\overline{\overline{(A + C)}}$ = (A + C) [0.5 pt]
Y = B + C [0.5 pt]
Z = $\overline{AY}$ [0.5 pt]
F = XZ [0.5 pt]

(B) Find a minimal implementation of the function below using only **2-input NAND gates**. *We will only accept circuit diagrams.* [6 pts]

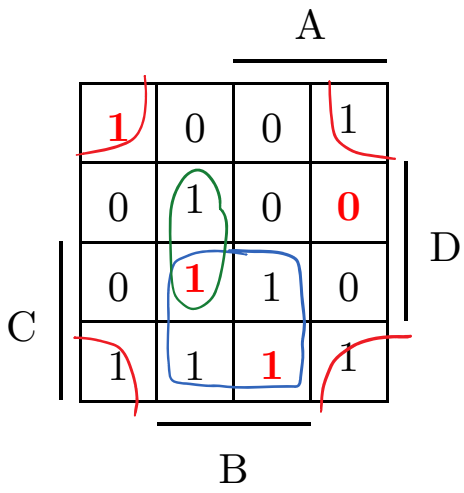
$$F = (\overline{A} + \overline{B})\overline{C} + D$$



[2 pt] Valid gate conversion from expression
[2 pt] DeMorgan's applications (either in expression or gates)
[2 pt] Conversion of extra NOTs to NANDs

Question 2: Karnaugh Maps [5 pts]

Find the *minimum sum-of-products solution* for the K-map shown below.

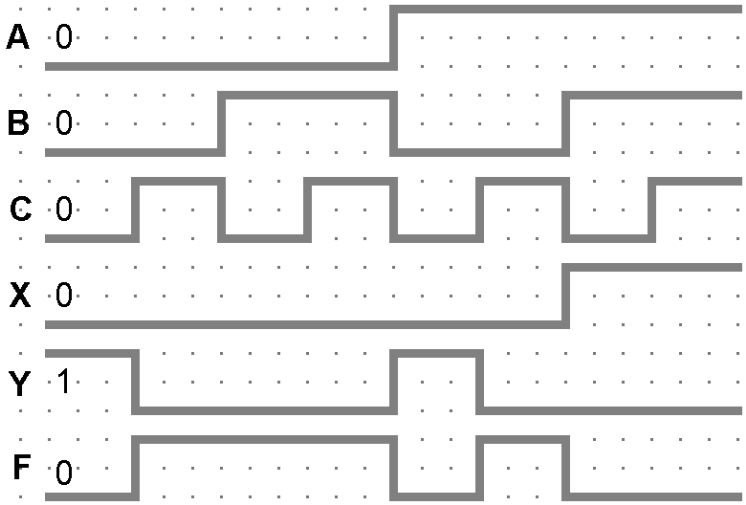


$= \overline{B}\,\overline{D} + BC + \overline{A}BD$

[2 pt] X choices
[1 pt each] correct term/grouping
[-0.5 pt each] smaller grouping used
[-0.5 pt each] extra grouping included

Question 3: Waveforms & Verilog [11 pts]

(A) Consider the Verilog simulated testbench waveforms shown. If we know that X and Y are outputs of 2-input logic gates, complete the module `Mystery` below. [5 pt]



For both X and Y:
[1 pt] Correct input signals
[1 pt] Correct gate used
Overall:
[1 pt] Correct Verilog syntax

```
module Mystery (F, A, B, C);
      output F;
      input  A, B, C;
      wire   X, Y;

      and  G1 (X, A, B); or assign X = A & B;

      nor  G2 (Y, B, C); or assign Y = ~(B | C);

      xnor G3 (F, X, Y);
endmodule
```

(B) We only have the 2-input logic gates at right available to us. Given the logic delays shown, draw out the circuit diagram of the *fastest* implementation of the Verilog statement below. [6 pts]

XOR	NAND	NOR
6 ns	8 ns	12 ns

Hint: Build a truth table first.

```
assign F = ~A & (A ^ B);
```

A	B	A^B	F
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

$F = \bar{A}B$