University of Washington – Computer Science & Engineering

Winter 2017 Instructor: Justin Hsia 2017-01-31

CSE 369 QUIZ 1

Name: _Perry_Perfect_____

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Please do not turn the page until 10:30.

Instructions

- This quiz contains 3 pages, including this cover page. You may use the backs of the pages for scratch work.
- Please clearly indicate (box, circle) your final answer.
- The quiz is closed book and closed notes.
- Please silence and put away all cell phones and other mobile or noise-making devices.
- Remove all hats, headphones, and watches.
- You have 20 minutes to complete this quiz.

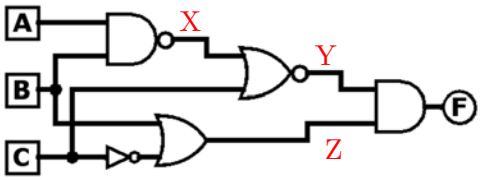
Advice

- Read questions carefully before starting. Read *all* questions first and start where you feel the most confident to maximize the use of your time.
- There may be partial credit for incomplete answers; please show your work.
- Relax. You are here to learn.

Question	Points	Score
(1) CL Gates	8	8
(2) K-map	5	5
(3) Waveforms & Verilog	11	11
Total:	**24**	**24**

Question 1: Combinational Logic Gates [8 pts]

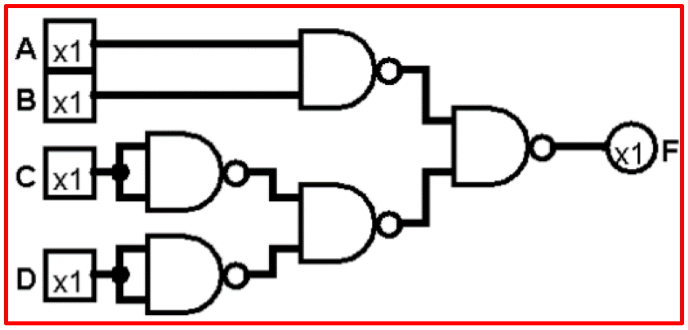
(A) Write out a Boolean expression for the circuit diagram below. *No need to simplify.* Remember to use + (OR), · (AND), and ¯ (NOT). [2 pts] $\mathbf{F = (\overline{AB} + C)(B + \bar{C})}$



X = $\overline{AB}$ [0.5 pt]
Y = $\overline{X + C}$ [0.5 pt]
Z = $B + \bar{C}$ [0.5 pt]
F = YZ [0.5 pt]

(B) Find a minimal implementation of the function below using only **2-input NAND gates**. [6 pts]

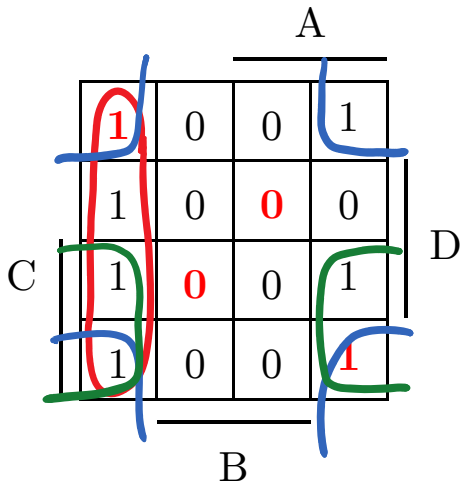
$$F = AB + (\overline{C + D})$$



[2 pt] Valid gate conversion from expression
[2 pt] DeMorgan's applications (either in expression or gate)
[2 pt] Conversion of extra NOTs to NANDs

Question 2: Karnaugh Maps [5 pts]

Find the *minimum sum-of-products solution* for the K-map shown below.

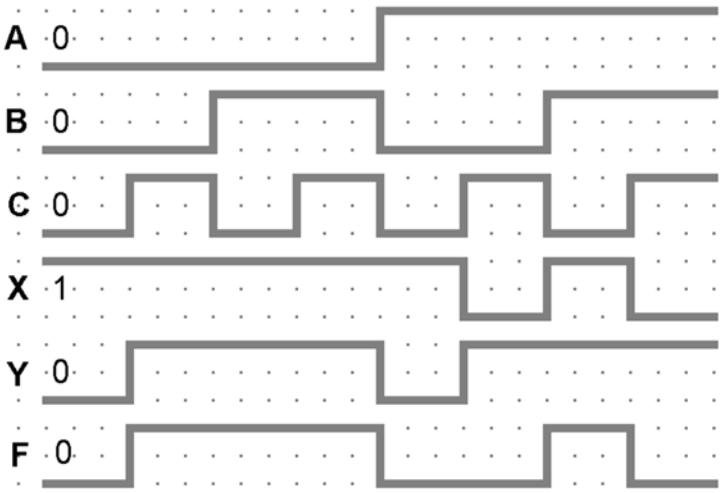


$\bar{A}\bar{B} + \bar{B}C + \bar{B}\bar{D}$
$= \bar{B}(\bar{A} + C + \bar{D})$

[2 pt] X choices: 1, 0, 0, 1
[1 pt each] correct term/grouping
[-0.5 pt each] smaller grouping used

Question 3: Waveforms & Verilog [11 pts]

(A) Consider the Verilog simulated testbench waveforms shown. If we know that X and Y are outputs of 2-input logic gates, complete the module `Mystery` below. [8 pt]

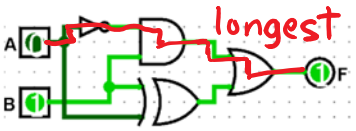


For both X and Y:
[2 pt] Correct input signals
[1 pt] Correct gate used
[1 pt] Correct Verilog syntax

```
module Mystery (F, A, B, C);
     output F;
     input  A, B, C;
     wire   X, Y;

     nand G1 (X, A, C); or assign X = ~(A & C);

     or   G2 (Y, B, C); or assign Y = B | C;

     and  G3 (F, X, Y);
endmodule
```

(B) Given the Verilog module `Circuit` below, assume that all gates (only 1- and 2-input) have a delay of 30 ns. If the values of inputs A and B first become known at $t = 0$ and output F is unknown at $t = 0$, at what time does F first become known? [3 pts]

```
module Circuit (F, A, B);
     output F;
     input  A, B;

     assign F = (~A & B) | (A ^ B);

endmodule
```



t = **90 ns**