University of Washington – Computer Science & Engineering
Winter 2020   Instructor: Justin Hsia   2020-02-04

CSE 369 QUIZ 1

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Please do not turn the page until 11:30.

Instructions

- This quiz contains 3 pages, including this cover page. You may use the backs of the pages for scratch work.
- Please clearly indicate (box, circle) your final answer.
- The quiz is closed book and closed notes.
- Please silence and put away all cell phones and other mobile or noise-making devices.
- Remove all hats, headphones, and watches.
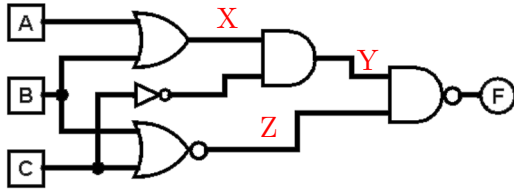- You have 20 minutes to complete this quiz.

Advice

- Read questions carefully before starting. Read *all* questions first and start where you feel the most confident to maximize the use of your time.
- There may be partial credit for incomplete answers; please show your work.
- Relax. You are here to learn.

Question	Points	Score
(1) CL Gates	8	8
(2) K-map	5	5
(3) Waveforms & Verilog	11	11
Total:	**24**	**24**

Question 1: Combinational Logic Gates [8 pts]

(A)   Write out a Boolean expression for the circuit diagram below. *No need to simplify.*
Remember to use $+$ (OR), $\cdot$ (AND), and $^{-}$ (NOT) as well as any necessary parentheses
to make your answer unambiguous. [2 pts] $\mathbf{F = \overline{(A + B)\overline{C}(B + C)}}$

$$X = A + B \qquad [0.5\ \text{pt}]$$
$$Y = \overline{B}X \qquad [0.5\ \text{pt}]$$
$$Z = \overline{B + C} \qquad [0.5\ \text{pt}]$$
$$F = \overline{YZ} \qquad [0.5\ \text{pt}]$$

(B)   Find a minimal implementation of the function below using only **2-input NOR gates**.
We will only accept circuit diagrams. [6 pts]
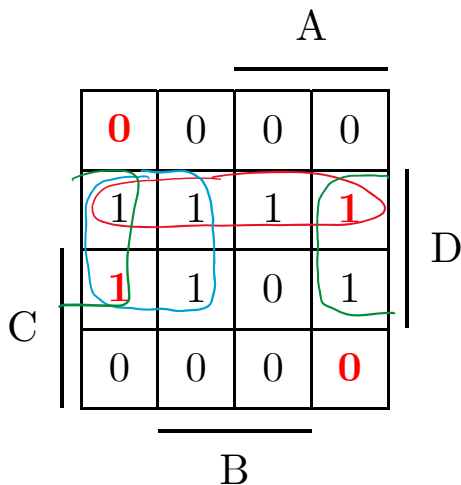
$$F = \overline{(A + B)\overline{\overline{C}}D}$$
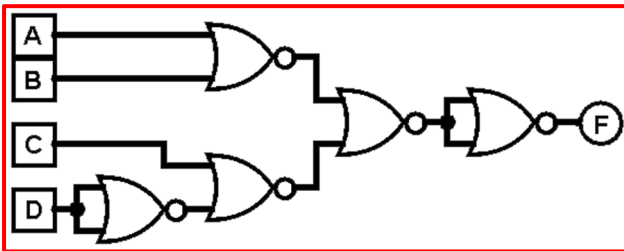
[2 pt] Valid gate conversion
from expression
[2 pt] DeMorgan's
applications (either in
expression or gates)
[2 pt] Conversion of extra
NOTs to NORs

Question 2: Karnaugh Maps [5 pts]

Find the *minimum sum-of-products solution* for the K-map shown below.

$$= \overline{C}D + \overline{A}D + \overline{B}D$$

[2 pt] X choices
[1 pt each] correct term/grouping
[-0.5 pt each] smaller grouping used
[-0.5 pt each] extra grouping included

Question 3: Waveforms & Verilog [11 pts]

(A) Consider the Verilog simulated testbench waveforms shown. If we know that X and Y are outputs of 2-input logic gates, complete the module `Mystery` below. [7 pt]
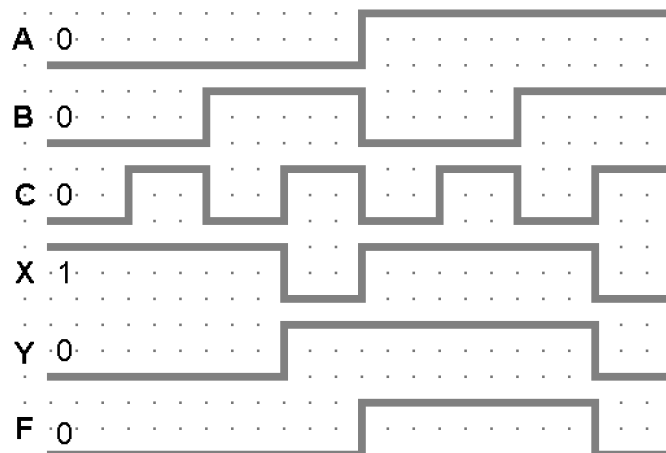
For both X and Y:
[2 pt] Correct input signals
[1 pt] Correct gate used
Overall:
[1 pt] Correct Verilog syntax


```verilog
module Mystery (F, A, B, C);
     output F;
     input  A, B, C;
     wire   X, Y;

     nand G1 (X, B, C); or assign X = ~(B & C);

     xnor G2 (Y, A, X); or assign Y = ~(A ^ X);

     and    G3 (F, X, Y);
endmodule
```

(B) The snippet below is from a Verilog testbench. Draw out the waveforms. [4 pts]

```verilog
logic [1:0] S;
initial begin
  S = 2'b00; #30; S[1] = 1; #10; S = S | 2'b01; #40;
  S = {S[0] ^ S[1], S[0] & S[1]}; #40;
end
```


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