CSE 369 QUIZ 1

Name: _____

Student ID
Number: _____

Please do not turn the page until 12:30.

Instructions
- This quiz contains 3 pages, including this cover page. You may use the backs of the pages for scratch work.
- Please clearly indicate (box, circle) your final answer.
- The quiz is closed book and closed notes.
- Please silence and put away all cell phones and other mobile or noise-making devices.
- Remove all hats, headphones, and watches.
- You have 20 (+5) minutes to complete this quiz.

Advice
- Read questions carefully before starting. Read *all* questions first and start where you feel the most confident to maximize the use of your time.
- There may be partial credit for incomplete answers; please show your work.
- Relax. You are here to learn.

Question	Points	Score
(1) CL Gates	8	
(2) K-map	5	
(3) Waveforms & Verilog	10	
Total:	23	

Question 1: Combinational Logic Gates [8 pts]

(A)   Write out a Boolean expression for the circuit diagram below. *No need to simplify.* Remember to use + (OR), · (AND), and ¯ (NOT) as well as any necessary parentheses to make your answer unambiguous. [2 pts]
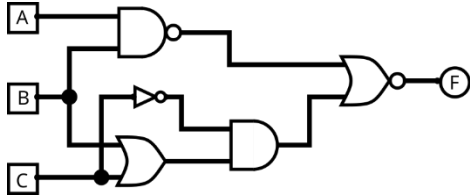
(B)   Find a minimal implementation of the function below using only **2-input NAND gates**. *We will only accept circuit diagrams.* [6 pts]
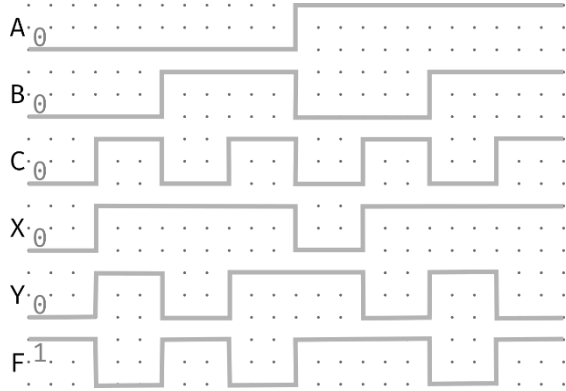
$$F = \overline{(\overline{A} + B)\overline{C}}$$

Question 2: Karnaugh Maps [5 pts]

Find the *minimum sum-of-products solution* for the K-map shown below.

Question 3: Waveforms & Verilog [10 pts]

(A)   Consider the Verilog simulated testbench waveforms shown. If we know that X and Y are outputs of 2-input logic gates, complete the module `Mystery` below. [7 pts]

A 0

B 0

C 0

X 0

Y 0

F 1.

```
module Mystery (F, A, B, C);
    output logic F;
    input  logic A, B, C;
    logic        X, Y;


    _____;


    _____;

    nand    G3 (F, X, Y);
endmodule
```

(B)   For the Verilog module `FastOrSlow` , assume the logic delays shown. If the values of A and B first become known at $t = 0$ and output F is unknown at $t = 0$, at what time is F first guaranteed to become known? *Remember to include units. The correct time is all that is required, but an incorrect answer can receive partial credit for correctly drawing the circuit diagram.* [3 pt]

NOT	AND	OR
10 ns	25 ns	20 ns

```
module FastOrSlow (F, A, B);
    output logic F;
    input  logic A, B;
    logic        W, X, Y, Z;

    and    G1 (W, A, B);
    not    G2 (X, B);
    or     G3 (Y, A, X);
    and    G4 (Z, W, Y);
    not    G5 (F, Z);
endmodule
```

$t =$