

CSE 369 QUIZ 2

Name: _____

Student ID
Number: _____

Please do not turn the page until 12:20.

Instructions

- This quiz contains 4 pages, including this cover page. You may use the backs of the pages for scratch work.
- Please clearly indicate (box, circle) your final answer.
- The quiz is closed book and closed notes.
- Please silence and put away all cell phones and other mobile or noise-making devices.
- Remove all hats, headphones, and watches.
- You have 30 (+5) minutes to complete this quiz.

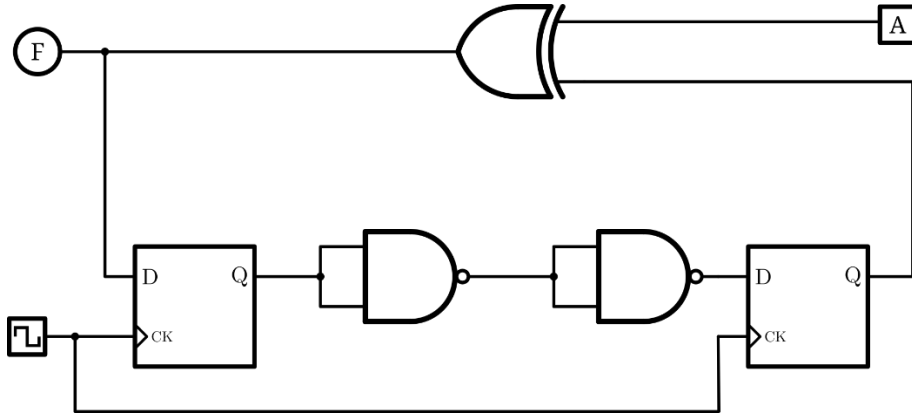
Advice

- Read questions carefully before starting. Read *all* questions first and start where you feel the most confident to maximize the use of your time.
- There may be partial credit for incomplete answers; please show your work.
- Relax. You are here to learn.

Question	Points	Score
(1) SL & Timing	6	
(2) FSM Implementation	10	
(3) FSM Design	12	
Total:	28	

Question 1: Sequential Logic & Timing [6 pts]

Consider the following circuit diagram with a clock period of **85 ns** (10^{-9} s), $t_{C2Q} = 25$ ns, $t_{XOR} = 25$ ns, and $t_{NAND} = 10$ ns. Assume that A changes **15 ns** after every clock trigger.

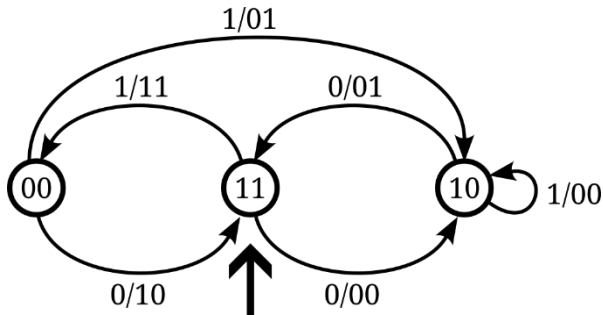


- (A) Calculate the **maximum setup time** that will allow the circuit to function correctly. Make sure to *include units*. [3 pts]

- (B) Calculate the **maximum hold time** that will allow the circuit to function correctly. Make sure to *include units*. [3 pts]

Question 2: Finite State Machine Implementation [10 pts]

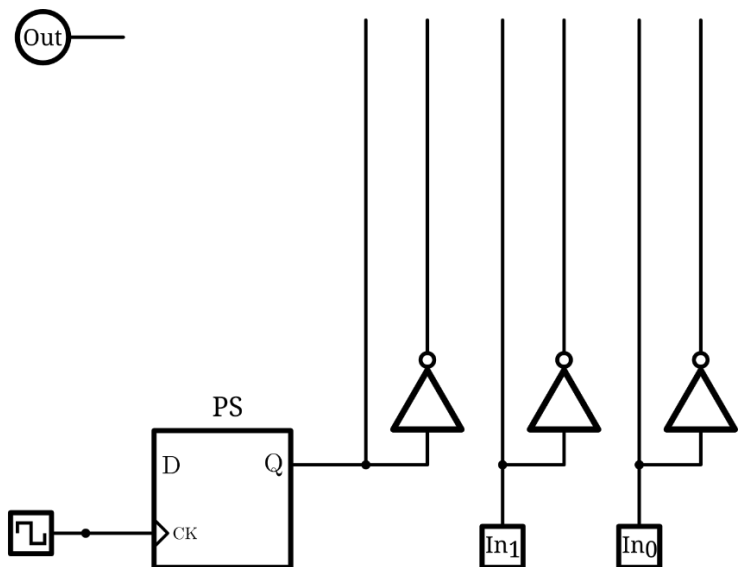
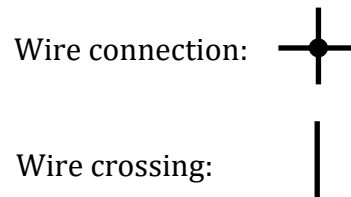
(A) Fill in the provided truth table based on the FSM shown. [2 pts]



PS ₁	PS ₀	In	NS ₁	NS ₀	Out ₁	Out ₀
0	0	0	1	1		0
0	0	1	1	0	0	1
0	1	0	X		X	
0	1	1	X	X	X	X
1	0	0		1	0	
1	0	1	1	0	0	
1	1	0	1	0	0	0
1	1	1		0	1	

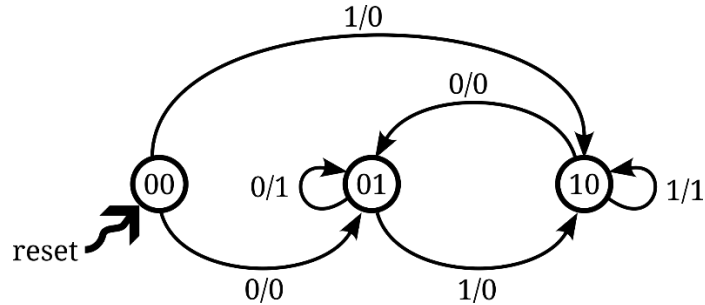
(B) Complete the circuit diagram below using *minimal logic* based on the truth table shown below. Use only 2-input logic gates. [8 pts]

PS	In ₁	In ₀	NS	Out
0	0	0	0	0
0	0	1	1	X
0	1	0	0	0
0	1	1	0	1
1	0	0	1	0
1	0	1	X	1
1	1	0	X	X
1	1	1	1	X



Question 3: Finite State Machine Design [12 pts]

The following FSM outputs a modified version of its stream of inputs:



- (A) Assume we pass the following stream of inputs (left-to-right) immediately after resetting the FSM. What is the corresponding stream of outputs? [4 pt]

Input: 1 0 1 1 1 0 0 0

Output:

- (B) As *briefly* as you can, describe how this FSM manipulates its input stream. [3 pt]

- (C) Complete the testbench `initial` block to test the state diagram as *thoroughly as possible*. You need to fill in all bolded blanks. You are welcome to fill out the Verilog comments to help you keep track of state, but these will not be graded. [4 pts]

```

initial begin
    In <= 0; // state: 00
    @(posedge clk); In <= _____; // state: _____
    @(posedge clk); In <= _____; // state: _____
    @(posedge clk); In <= _____; // state: _____
    @(posedge clk); In <= 0; // state: _____
    @(posedge clk); $stop();
end
  
```

- (D) What transition of the state diagram were you not able to test in the above testbench? [1 pt]