467 Advanced Digital Design

Instructor
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Office hours: TBA

Teaching Assistant
Doug Beal
Sieg X
Office hours: TBA

Topics to be covered: Advanced techniques in the design of digital systems, Hardware description languages, combinational and sequential logic synthesis and optimization methods, partitioning, mapping to regular structures, emphasis on reconfigurable logic as an implementation medium, memory system design, digital communication including serial/parallel and synchronous/asynchronous methods.

Prerequisites: CSE370 and CSE326. It is not required, but having taken 378 will be helpful. Additionally since we are focusing on graphics this quarter (see project below), having taken 457 is helpful. I want to stress, however, that *no prior knowledge* of graphics is required or expected. The first project is intended to teach you everything you will need to know about graphics for this class (basically the first weak of 457).

Course Goals: To provide in-depth understanding of digital systems and their design, from specification and simulation to construction and debugging.

Textbook: We will be using: Fundamentals of Digital Logic with Verilog Design. This textbook is the same as the one that will be used in 370 *in the future*. Unfortunately, since this switch was just made it probably means you need to purchase this book new for this class.

Web page: www/467. You should read the webpage often enough. Stuff will be there.

Grading: Project 50%, "Optional" Final 40%, Participation 10%. Note, you can only receive a 3.8 or 4.0 in this class if you complete the project and it works. In addition, if your lab grade is greater than or equal to 3.8 (out of 4.0) you will not need to take the final.

Projects: This is a lab class. You will be spending *significant* in-class and out of class time in the hardware lab (Sieg X). The lab project will be time consuming and in light of this there will be no other homework (normally this class would have weakly homework as well as labs) and no exams (if you do well in the project). You must work in a group of 2 for the lab project. Your partner must be in the same lab section. I realize that some of you would prefer to work alone, but you must work with a partner because we have only so many prototype boards.

The hardware projects will be challenging, but I hope a lot of fun too. This quarter this class is going to have a theme to its projects. The theme is high-end consumer graphics hardware. Each of the projects will build upon the prior ones and eventually we will have constructed a 3D pipelined graphics card. Here is a broad list of projects we will be doing: (1) construct 3D hardware simulator, (2) build RAMDAC and framebuffer, (3) build 2D rendering hardware, (4) build 3D rendering hardware, (5) pipeline 3D rendering hardware, and possibly (6) to be

determined (likely will be something of your own choosing to build on/advance your 3D hardware.

Bruce Hemmingway is the lab manager. Follow his directions at all times. He has extensive experience (*far more than me or the TA's*) in industry and has built many of the circuits (and variations there of) that you will be doing for this class. There are some standard lab policies the department follows that Bruce can explain better the first day of lab.

Project grading: Projects will be graded on whether or not they work, their elegance, and on a one-on-one interview. This interview is conducted individually (not in project pairs). You are responsible for knowing about all aspects of the project, even those that your partner undertook. The interview will focus on that part of the project you did, however. <u>You and your partner may not receive the same grade on the project.</u>

Collaboration: I encourage you to help out other students. Sometimes it just takes another pair of eyes to catch the bug in the wiring. However, there is a line between assisting and actually doing the project for them. Do not cross that line.

Late Policy: You can turn projects in 1 day late for any reason. You must send an excuse, however, prior to the actual turn in time, to myself at the TA. This excuse does not have to be true, but untrue excuses should at least be funny. Example: "My chihuahua ate my parrot and I was too depressed do work."