High-speed signaling

- Delays
- Transmission lines
- Ringing and terminations
- Pin inductance
- Tips and suggestions

What does high-speed mean?

Abstractions in digital design

1. Digital interpretation of analog values
   - Transistors as switches
   - Analog voltages as "1s" or "0s"
2. Logic devices as idealized Boolean primitives
   - Switches as logic elements
   - Ignore electrical characteristics of devices, wire, etc.
3. Steady-state abstraction
   - Combinational: Outputs depend on inputs *after a sufficient time*
   - Sequential: Outputs retain their *settled state*
     - Clock hides transient behavior
4. Finite-state behavior of sequential systems

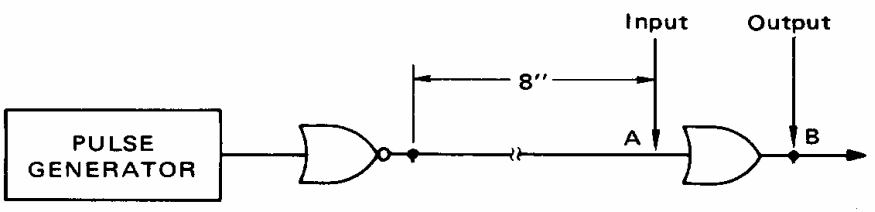
Definition of "high speed"

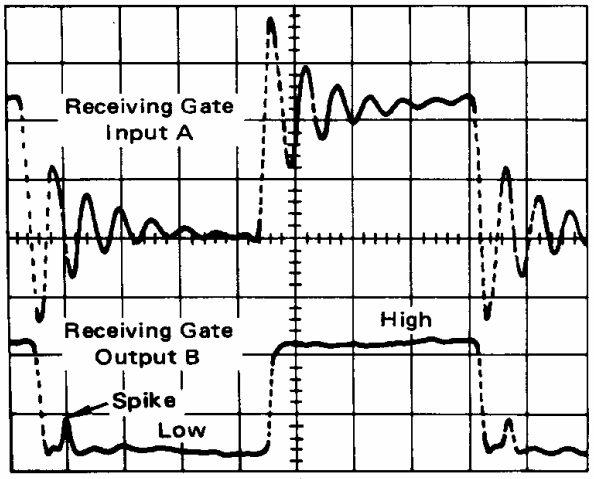
The speed at which one or more digital abstractions fail, as a direct consequence of the circuit speed

- Speed ≡ Clock frequency and/or edge rates
- Typical problems
  - Logic gates or flip-flops don't have time to settle
  - Clock skew causes races
  - Wire (interconnect) acts like transmission lines

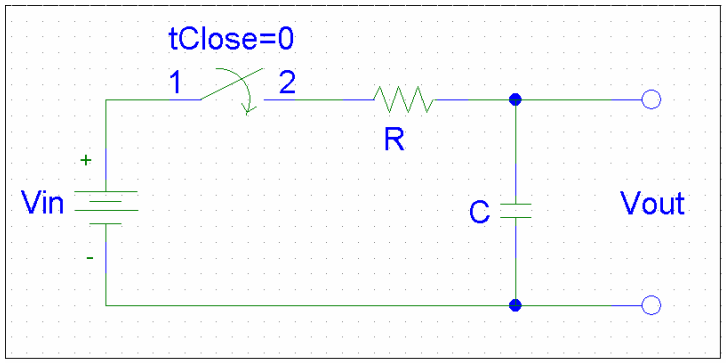
When wire isn't...

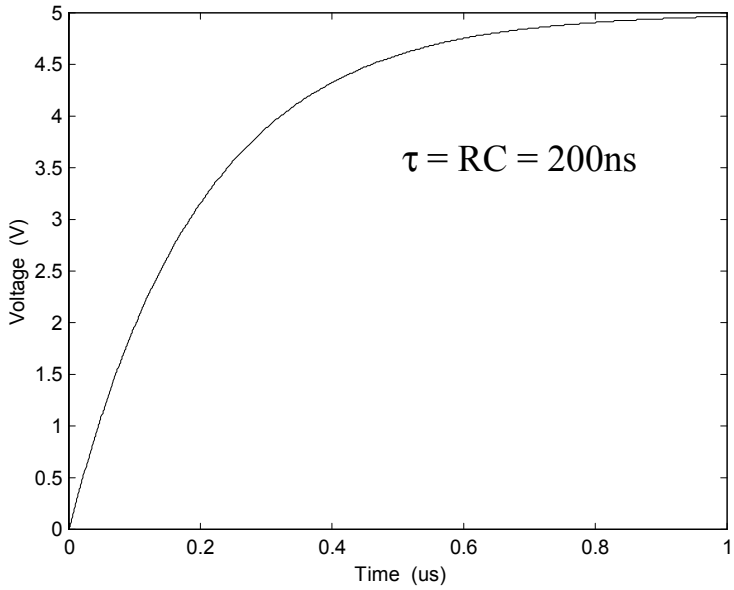
- ***All*** wires are transmission lines
  - Just like all voltages are analog
- Past: Signals on PCBs were slow
  - Wire delays were small compared with signal risetimes
  - Wires passed digital voltages unchanged
- Today: PCB design requires transmission-line analysis
  - Wire delays are long compared with signal risetimes
  - Wires don't pass digital voltages unchanged





Background: Time constants





$$V_{\text{in}} = v_r + V_{\text{out}} \qquad v_r = iR \qquad i = C\frac{dV_{\text{out}}}{dt}$$

$$V_{\text{in}} = iR + V_{\text{out}}$$

$$V_{\text{in}} = RC\frac{dV_{\text{out}}}{dt} + V_{\text{out}}$$

$$-RC\,dV_{\text{out}} = \left(V_{\text{out}} - V_{\text{in}}\right)dt$$

$$-\frac{dt}{RC} = \frac{dV_{\text{out}}}{\left(V_{\text{out}} - V_{\text{in}}\right)}$$

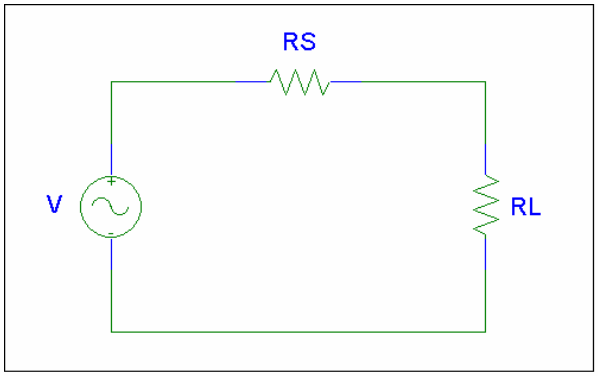
$$-\frac{1}{RC}\int_0^t dt = \int_0^{v_{out}(t)} \frac{dV_{\text{out}}}{\left(V_{\text{out}} - V_{\text{in}}\right)}$$

$$-\frac{t}{RC} = \ln\left(V_{\text{out}}(t) - V_{\text{in}}\right) - \ln\left(-V_{\text{in}}\right)$$

$$V_{\text{out}}(t) = V_{\text{in}}\left(1 - e^{-\frac{t}{RC}}\right)$$

Background: Maximum power transfer

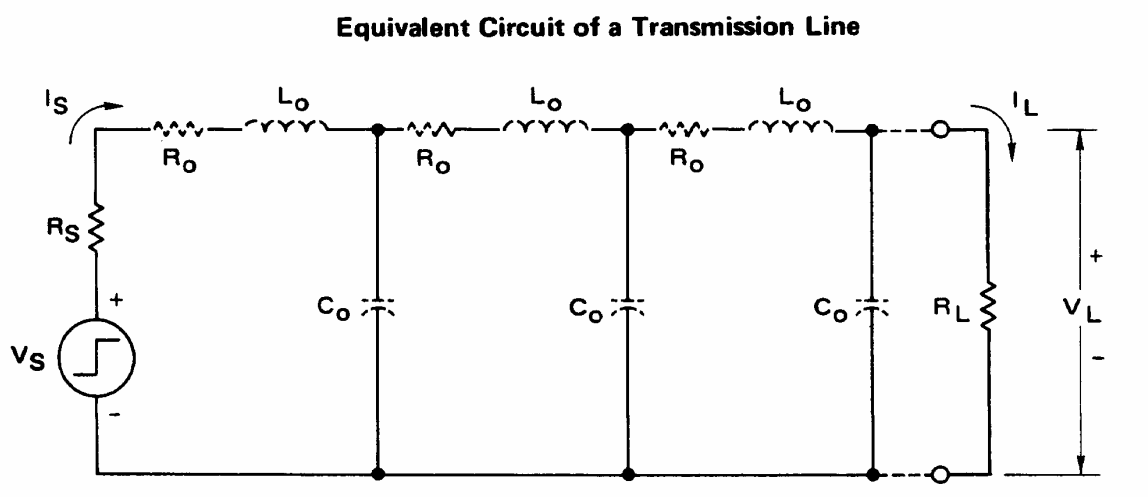
- How much power do you transfer to R_L?
  - Transfer zero power when $R_L = 0$
  - Transfer zero power when $R_L = \infty$
  - Transfer maximum power when $R_L = R_S$



- Our problem: R_s is a transmission line (a wire)
  - Transfer maximum power when R_L = wire impedance
  - Else some power is returned to the voltage source

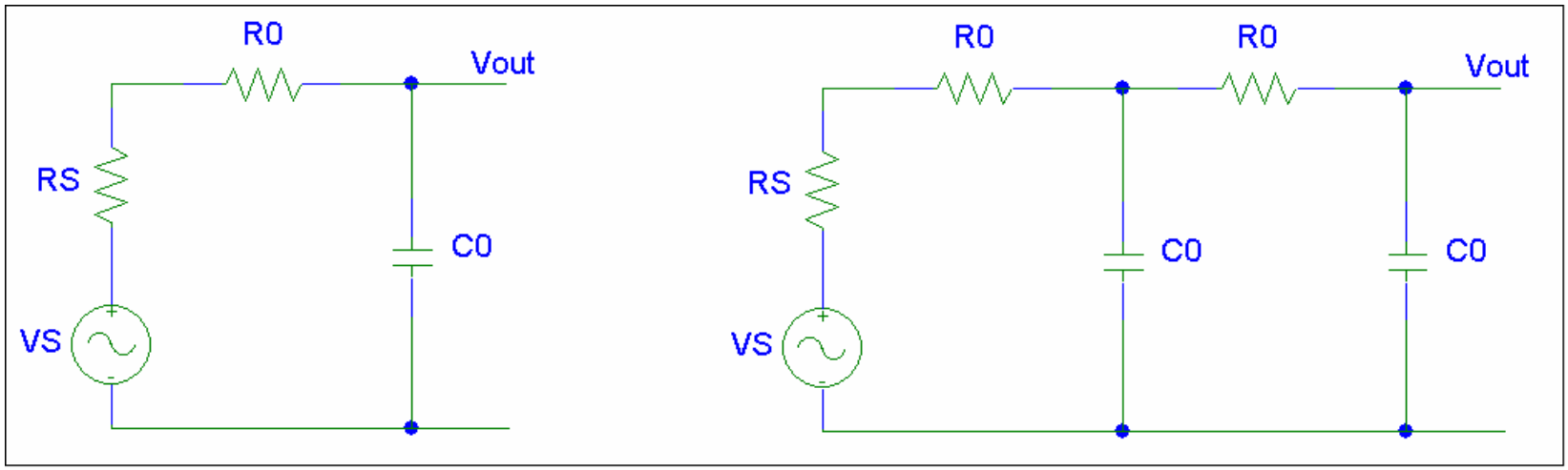
Transmission-line model

- This is a model of a wire (an abstraction)
  - Adequate when dispersion is low



- Cases
  1) R_0, C_0, L_0 are small: Treat wire as ideal
  2) R_0, L_0 are small: Treat wire as lumped capacitance
  3) L_0 is small: Treat wire as distributed RC
  4) None are small: Treat wire as transmission line

Cases 2, 3: RC models



$$R_0 << R_S$$

$$V_{out} = 1 - e^{-t/RC}$$

Where R is the total resistance
C is the total capacitance
Wire is short (defined later)

$$R_0 \sim R_S$$

$$V_{out} = 1 - e^{-2t/R_0 C_0 l^2}$$

Where ℓ is the length of the wire
R0 is resistance per unit length
C0 is capacitance per unit length
R0 dominates inductance L

Case 4: Transmission-line model

- Problem: Signal risetime is faster than the wire delay
  - Inductance L limits the propagation velocity by V=L(dI/dt)
- Thought process: We won't see ringing if it occurs entirely during the signal's rising or falling edge
- Assume a simple wire
  - Require $\text{length}_{max} < \frac{t_r}{2t_{pd}}$ or $\text{delay}_{max} < \frac{t_r}{2}$
  - Where $t_r \equiv$ rise time
  - $t_{pd} \equiv$ delay per unit length
  - length ≡ length of wire
  - delay ≡ wire delay = $t_{pd} \times$ length

The factor of 2 accounts for the fact that the signal has to travel to the end of the wire, then return on the ground plane

Some definitions

- $t_{pd} = \sqrt{L_0 C_0}$ in ns/ft
  - The signal propagation time
- $Z_0 = \sqrt{\frac{L_0}{C_0}}$ in Ohms
  - The impedance of a transmission line
- How to find C_0 and L_0?
  - Use an LCR meter
  - Use an EM simulator

L_0 is inductance per unit length

C_0 is capacitance per unit length

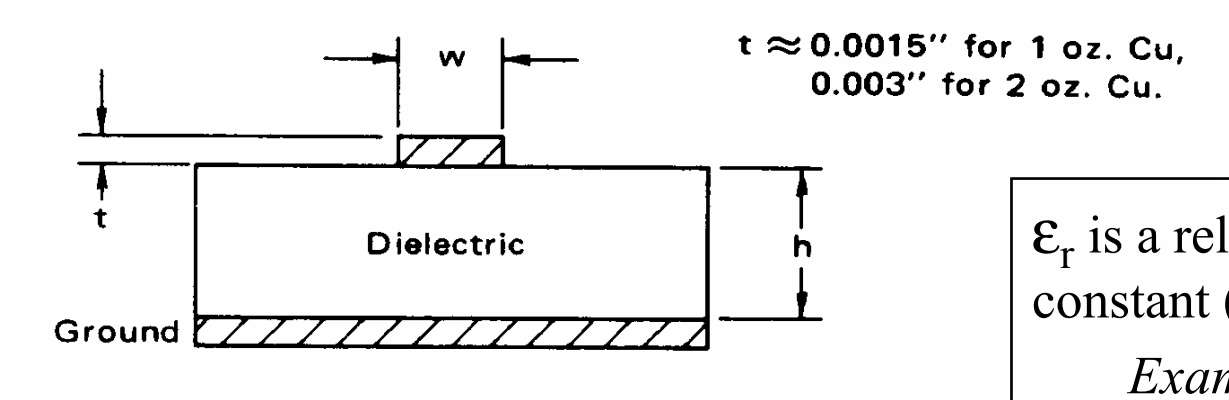
Most PCB vendors will size traces for you

You just tell them Z_0

Microstrip: Wire over a plane

$$Z_0 = \frac{87}{\sqrt{\varepsilon_r + 1.41}} \ln\left(\frac{5.98h}{0.8w + t}\right) \quad \text{Ohms}$$

$$t_{pd} = 1.017\sqrt{0.475\varepsilon_r + 0.67} \quad \text{ns/ft}$$



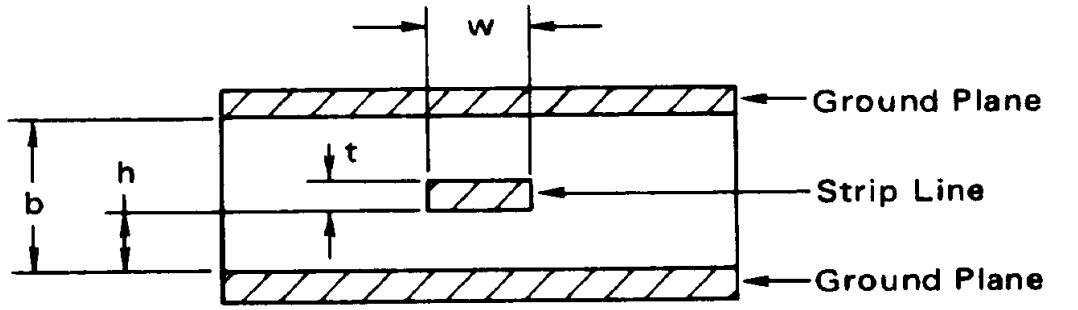
ε_r is a relative dielectric constant (ref to vacuum)

Example: $\varepsilon_r = 4.8$ for FR-4 epoxy-glass

Stripline: Wire sandwiched between planes

$$Z_0 = \frac{60}{\sqrt{\varepsilon_r}} \ln\left(\frac{4b}{0.67\pi w\left(0.8 + \frac{t}{w}\right)}\right) \quad \text{Ohms}$$

$$t_{pd} = 1.017\sqrt{\varepsilon_r} \quad \text{ns/ft}$$



Tip: Planes can be power *or* ground

Loading a line

- Attaching logic gates to a line increases the capacitance
  - Where $C_d \equiv$ Capacitive load on transmission line

$$Z_0' = \frac{Z_0}{\sqrt{1 + \frac{C_d}{C_0}}}$$

$$t_{pd}' = t_{pd}\sqrt{1 + \frac{C_d}{C_0}}$$

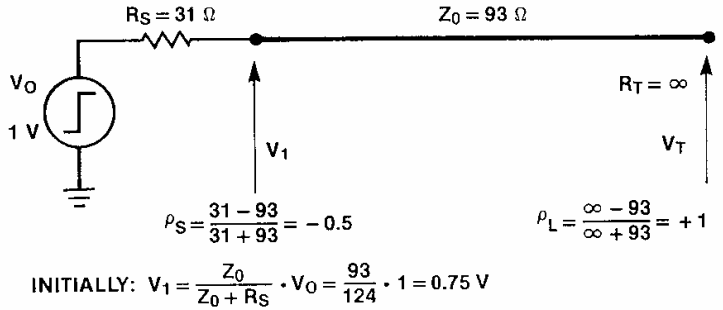
What if we violate the limit?

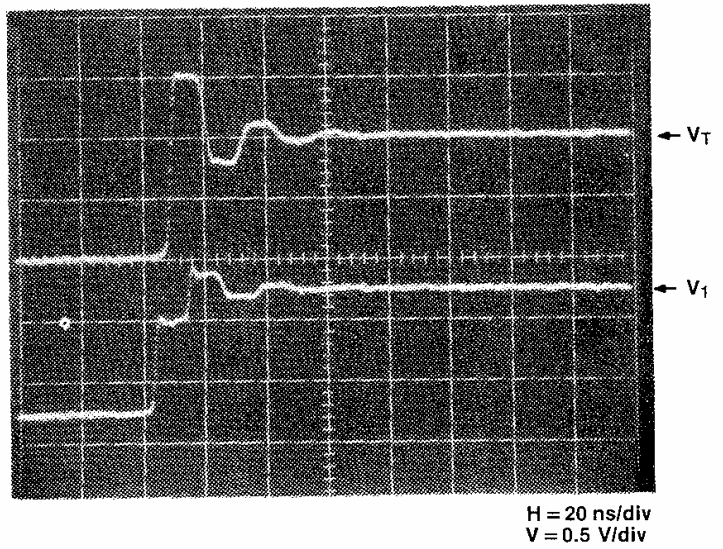
- Get overshoot/undershoot and reflections
  - Signal bounces back and forth between the ends of the line
  - Bounce gets reduced by a factor ρ at each reflection

$$\rho_S = \frac{R_S - Z_0}{R_S + Z_0}$$

$$\rho_L = \frac{R_L - Z_0}{R_L + Z_0}$$

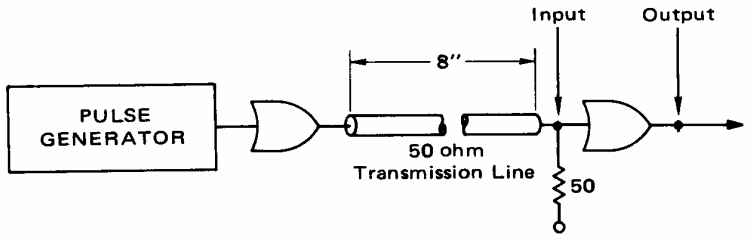
Fig. 4-3 Multiple Reflections Due to Mismatch at Load and Source



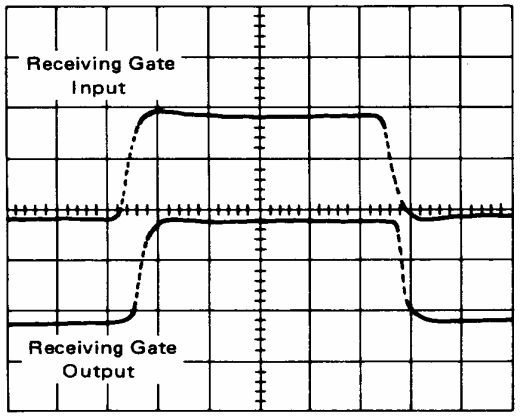


Terminating transmission lines: Option1

- Terminate line into an equivalent load
  - Advantages
    - Can distribute gates along line
  - Disadvantages
    - Driver consumes lots of power
    - Driver has large output currents
    - Driver has large transients
- Note: Properly terminated lines look like purely resistive loads



(a) Test Configuration

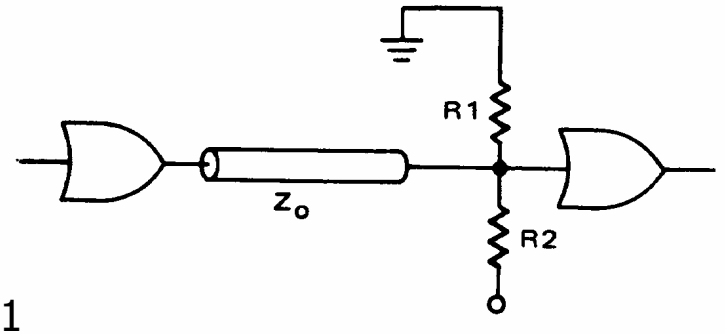


Horizontal Scale = 10 ns/cm

(b) Input and Output Waveforms

Terminating transmission lines: Option2

- Terminate the line into a Thevenin equivalent load
  - Termination as good as option1
  - Advantages
    - Can distribute gates along line
    - Smaller peak output current than option1
    - Smaller driver transients than option1
  - Disadvantages
    - Same total power as option1
    - Need to set DC bias at logic threshold



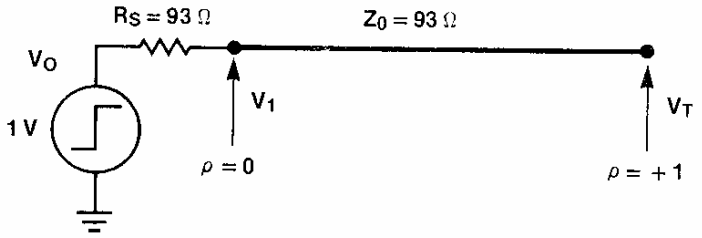
$$R_L = \frac{R_1 R_2}{R_1 + R_2}$$

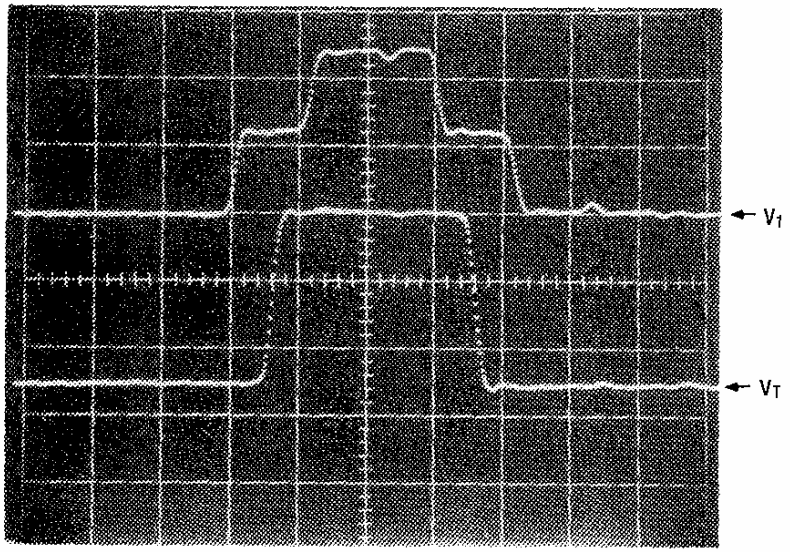
Terminating transmission lines: Option3

- Series terminate the line
  - Termination inferior to option1
  - Advantages
    - No static power consumption
    - Can drive many loads
  - Disadvantages
    - Half-amplitude transients on line
    - Cannot place gates along line (only place gates at ends)

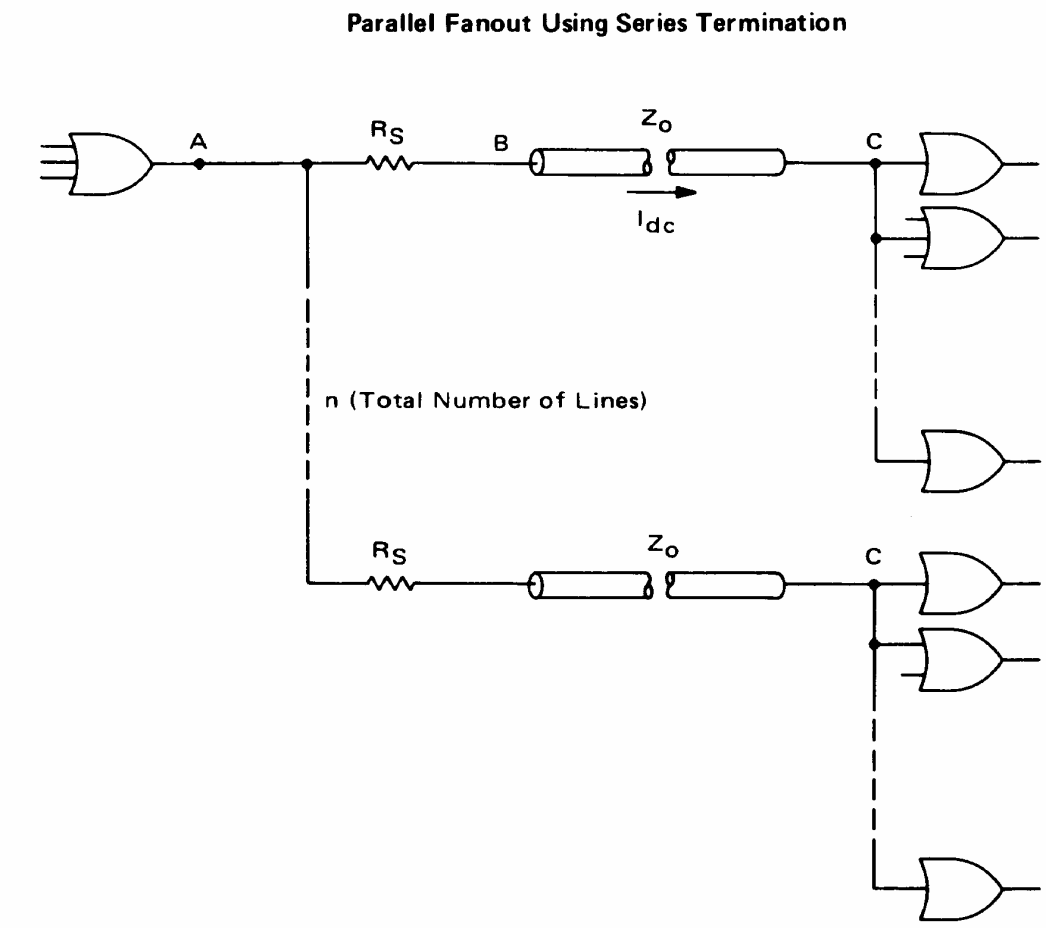
Tip: Z_{wire} ~ 100–140 Ohms (assuming no ground plane)

Fig. 4-7 Series Terminated Line and Waveforms



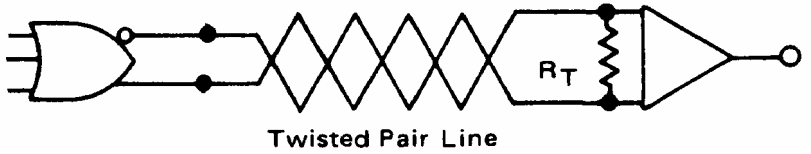


Driving multiple loads using option3



Terminating transmission lines: Option4

- Differentially terminate the line
  - Termination as good as option1
  - Advantages
    - Can distribute gates along line
    - Differential signals
    - Low crosstalk
    - Don't need contiguous ground plane
  - Disadvantages
    - High driver power
    - Need differential receivers



- Note: Great for buses
  - Put terminations at both ends of bus
  - SCSI uses this approach

Issues

- Rule was: $\text{length}_{max} < \frac{t_r}{2t_{pd}}$ or $\text{delay}_{max} < \frac{t_r}{2}$
- But...
  - Series terminated lines have accelerated rise times
    - Voltage doubles at line end
  - Analysis shows 15% overshoot/undershoot
    - Assumes accurate calculations…
- Instructor experience: This rule is not conservative enough

A more conservative rule

- **Rule:** $\text{length}_{max} < \frac{t_r}{4t_{pd}}$ or $\text{delay}_{max} < \frac{t_r}{4}$
  - Where $t_r \equiv$ rise time
  - $t_{pd} \equiv$ delay per unit length
  - length $\equiv$ length of wire
  - delay $\equiv$ wire delay = $t_{pd} \times$ length
  - Use t'_{pd} when line is loaded

Back of the envelope calculations

- Estimate the wire delay in ns
  - Twisted pair: ~ 8.5 in/ns
  - Coaxial cable: ~ 8 in/ns
  - Microstrip: ~ 7 in/ns
  - Stripline: ~ 5.5 in/ns

  Assuming FR-4
- Check if the wire is short
  - $\text{delay} < \frac{t_r}{4}$???
  - If yes, wire will act like wire
    - You are safe
  - If no, wire may act like a transmission line
    - Do more analysis

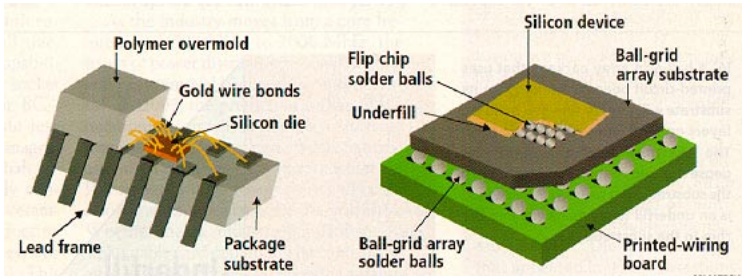
Example:
1ns risetime
5in trace over gnd

Delay = 5/7 ns
$t_r/4$ = 1/4 ns

5/7 > 1/4
$\Rightarrow$ You are not safe

Tip: Pin inductance and I/O speed

- Rule of thumb: $t_{r\_min} > \frac{5L}{Z_0}$
  - t_{r_min} is minimum signal rise time
  - L is pin inductance
  - Z_0 is trace impedance
  - Example:
    - L = 5nH
    - Z_0 = 50 Ohms
    - t_{r_min} = 500psec



Tips for series terminations

- Use a series resistor for each load
  - Drive all loads in parallel
- Do not daisy-chain loads
  - Half-amplitude voltage swings on the wire
- Reduce R_s by 33%
  - Example: If Z=50, choose R_s = 33 Ohms
    - Driver has a finite source impedance
    - Line loads cause Z↓
    - Slight overshoot is good (fast edges)

Tips for minimizing reflections

- Reduce signal rise times
  - Example: Xilinx has selectable output rise times
- Reduce line lengths
- Terminate long lines properly
- Use contiguous ground or power planes
  - Under transmission lines
  - Or use differential terminations
- Avoid sharp bends in wires
  - Curves are better than corners

Tips for routing traces on PCBs

- Use differential wires to communicate between systems
  - Or through card-edge connectors
- Use ground & power planes
  - Low-Q decoupling capacitors between them
  - Avoid cuts in ground plane
    - esp. under controlled-impedance traces
- Avoid long parallel wires
  - Unless they are differential
  - Using ground between traces reduces crosstalk

Tips for ground planes

- The width of a ground plane must be 3× the width of the controlled impedance trace
  - Do not put cuts in the ground plane
  - Put ground plane directly under trace