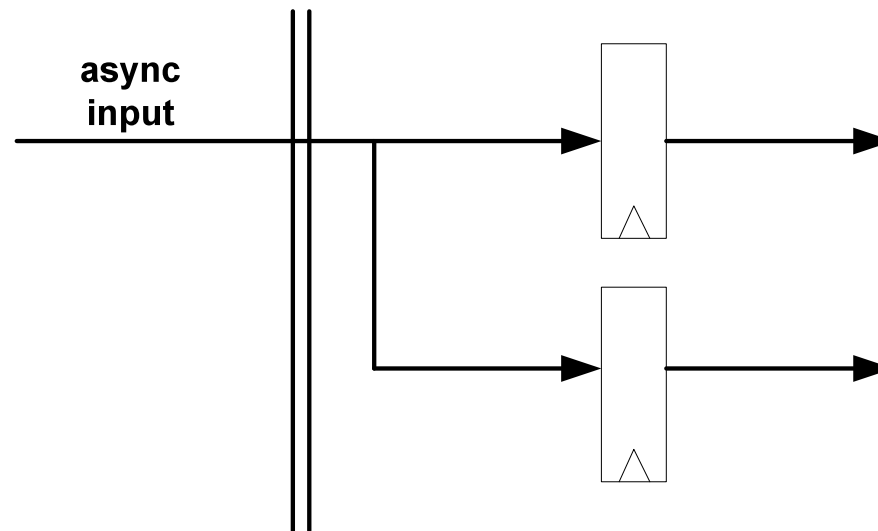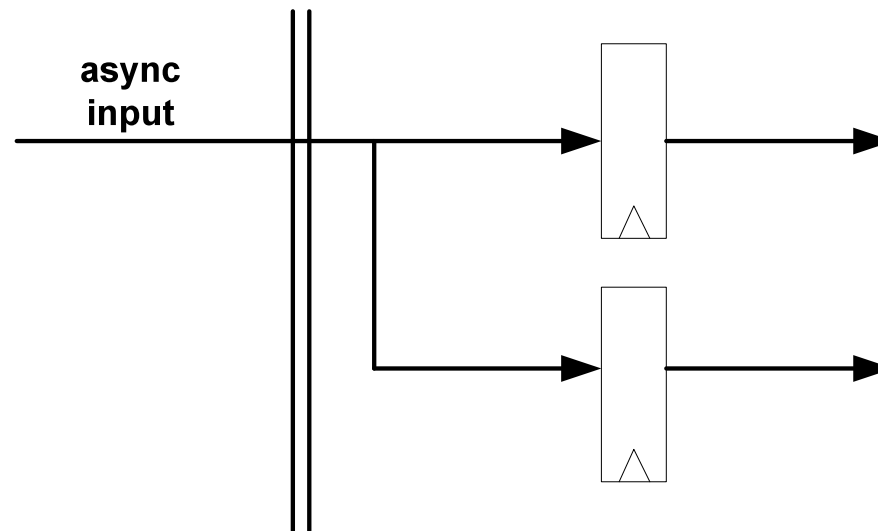# The Primary Problem with Asynchronous inputs

- What goes wrong here? (Hint: it's not a metastability thing)

ANOTHER PROBLEM WITH ASYNCHRONOUS INPUTS

- What goes wrong here? (Hint: it's not a metastability thing)
  - Slight delay differences mean that the registers can disagree on the input value
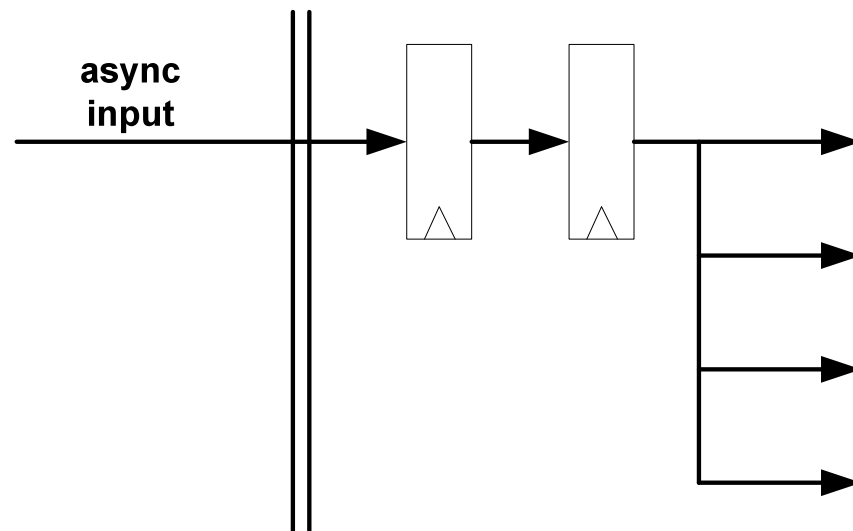 - "Inconsistent value problem"

MORE ASYNCHRONOUS INPUTS

- What is the problem?

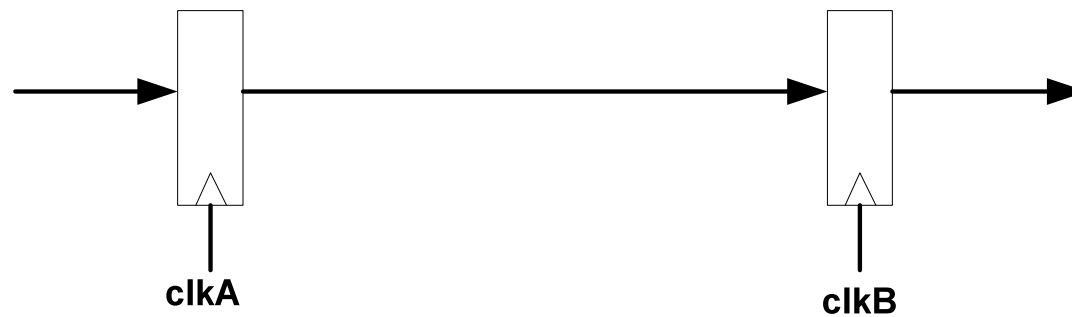- "Inconsistent value problem"
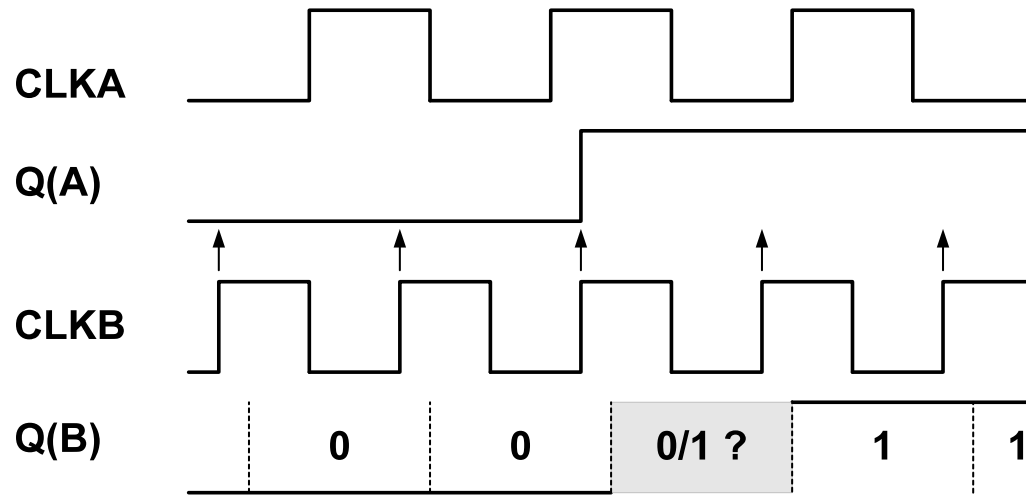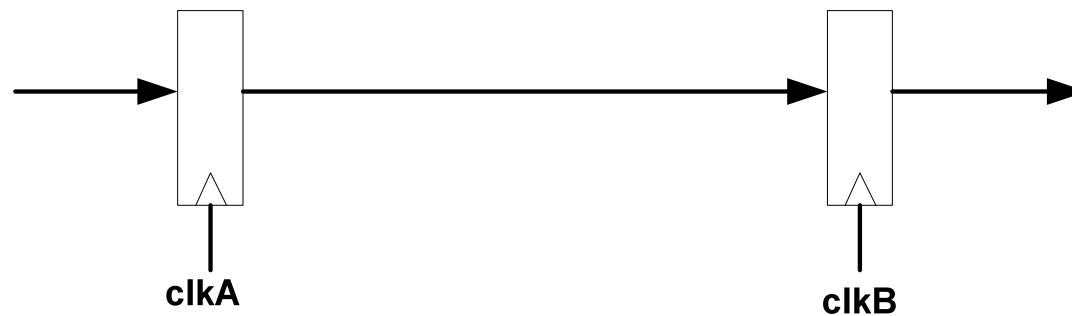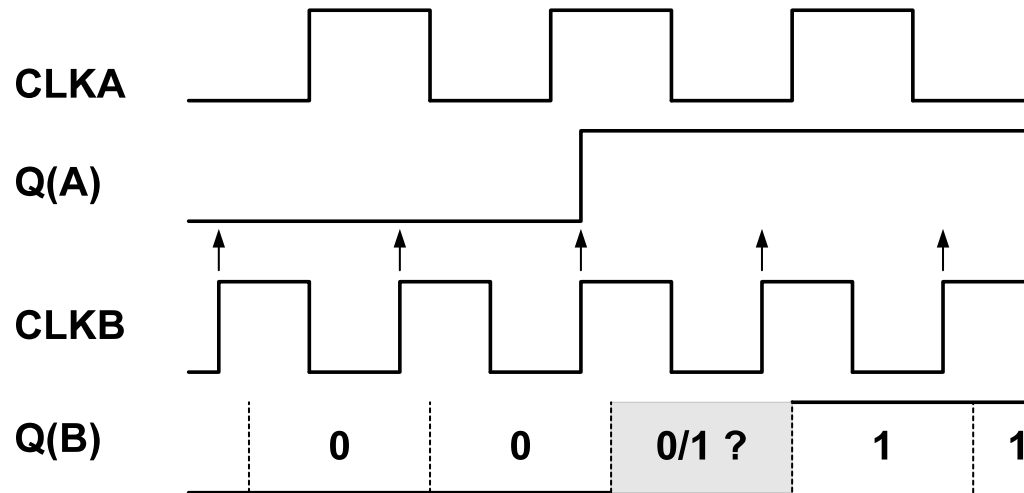 - Two paths from input to two different registers
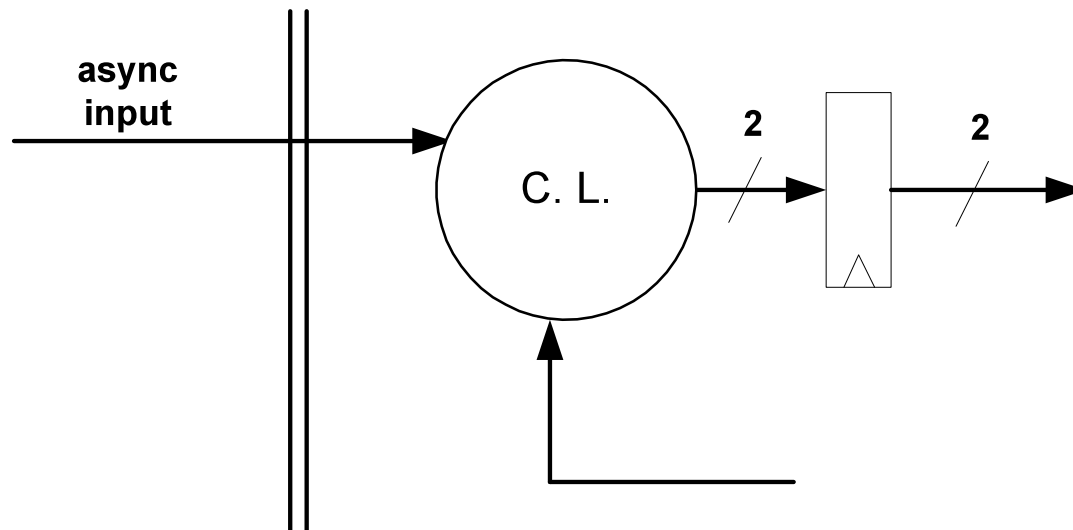
Important Rule!

- Exactly one register makes the sampling decision
    - Where it enters the clock domain
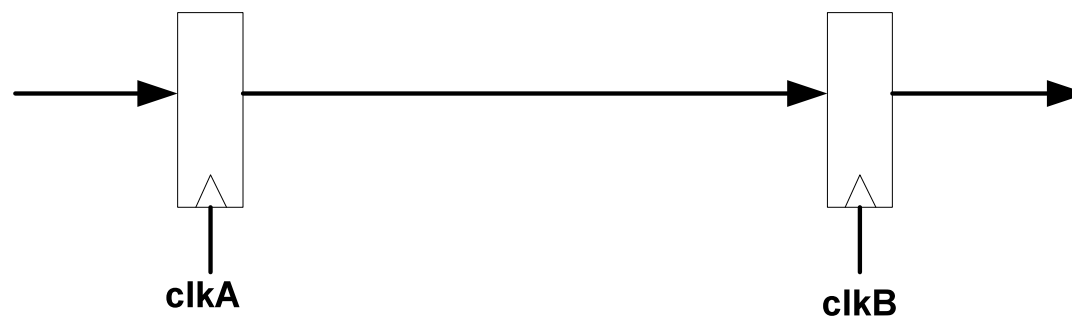   - Completely solves the "inconsistent value problem"

async
input
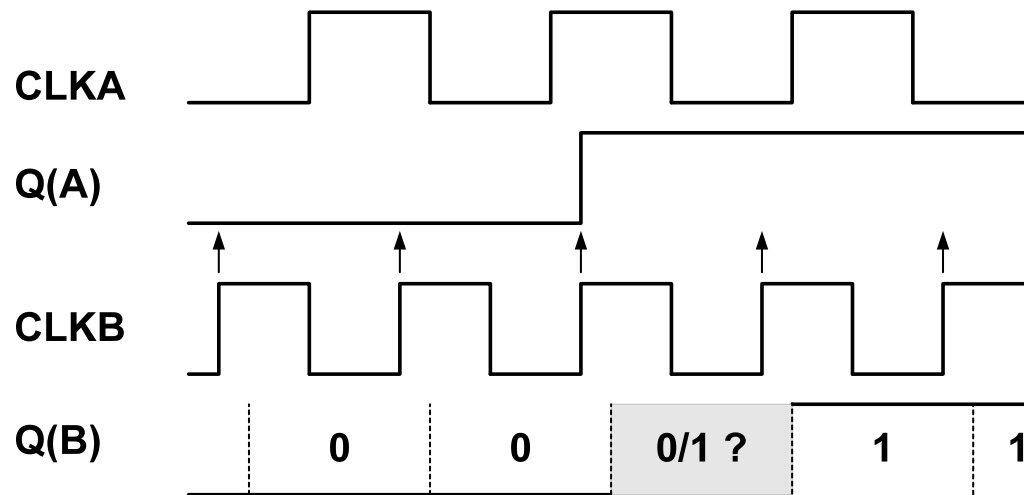
Sampling external inputs

CLKA

Q(A)

CLKB

Q(B) 0 0 0/1 ? 1 1

clkA

clkB

Doesn't matter which the register decides
There is a clean 0 -> 1 on the input

CLKA

Q(A)

CLKB

Q(B) | 0 | 0 | 0/1 ? | 1 | 1

clkA

clkB

Problem: Register sometimes can't decide
The Metastability problem

CLKA

Q(A)

CLKB

Q(B)   0   0   0/1 ?   1   1
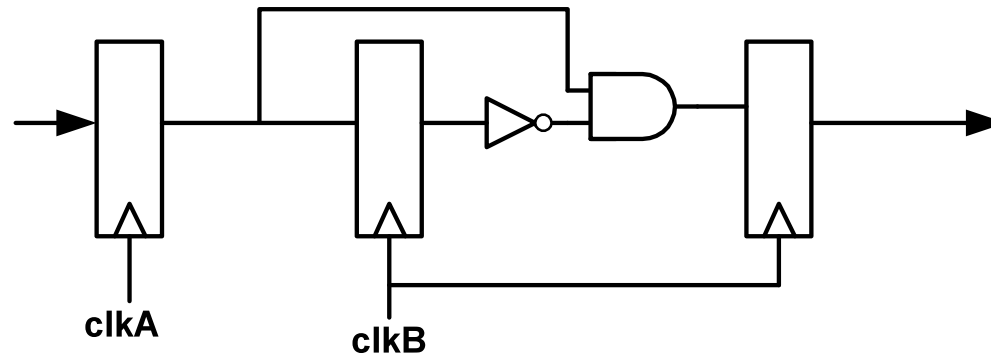
clkA

clkB

"SYNCHRONIZER"

- We sample with a register pair

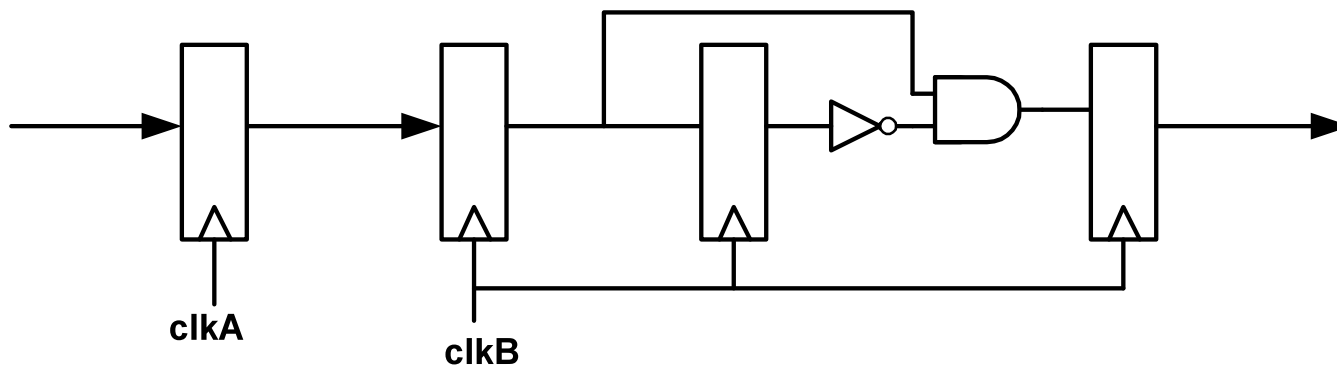- Maximizing the resolution time
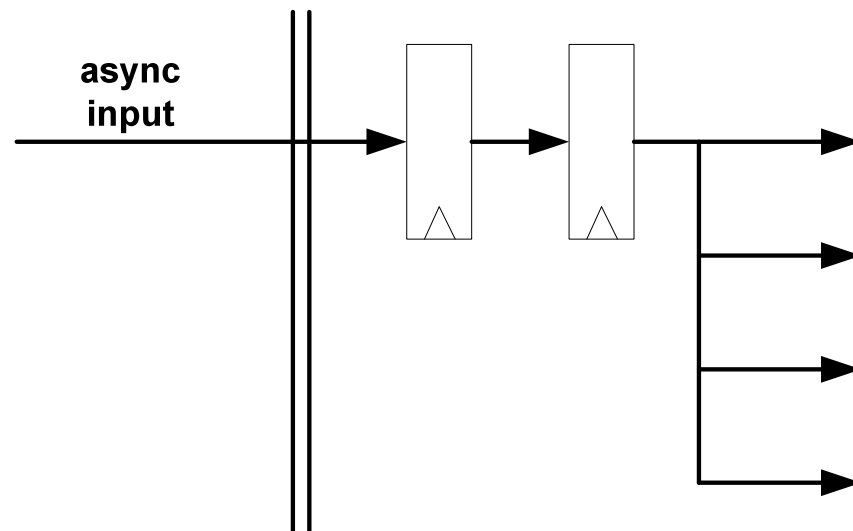
WHAT DOES THIS CIRCUIT TRYING TO DO?
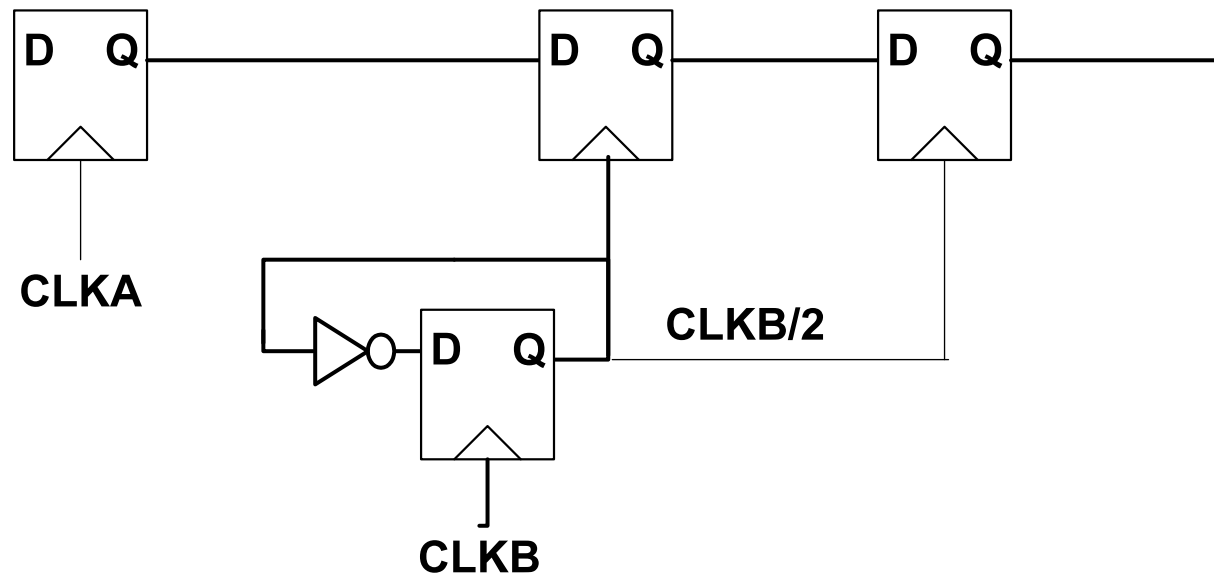
- What's wrong with it?

TWO REGISTERS BEFORE WE USE THE SIGNAL
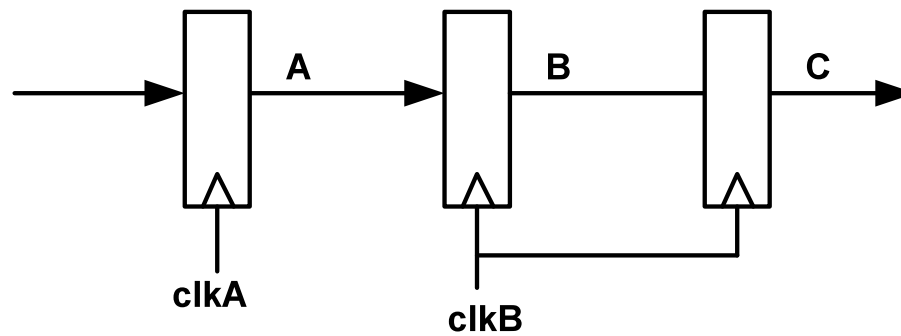
- How much better is this?

STRETCHING THE RESOLUTION TIME
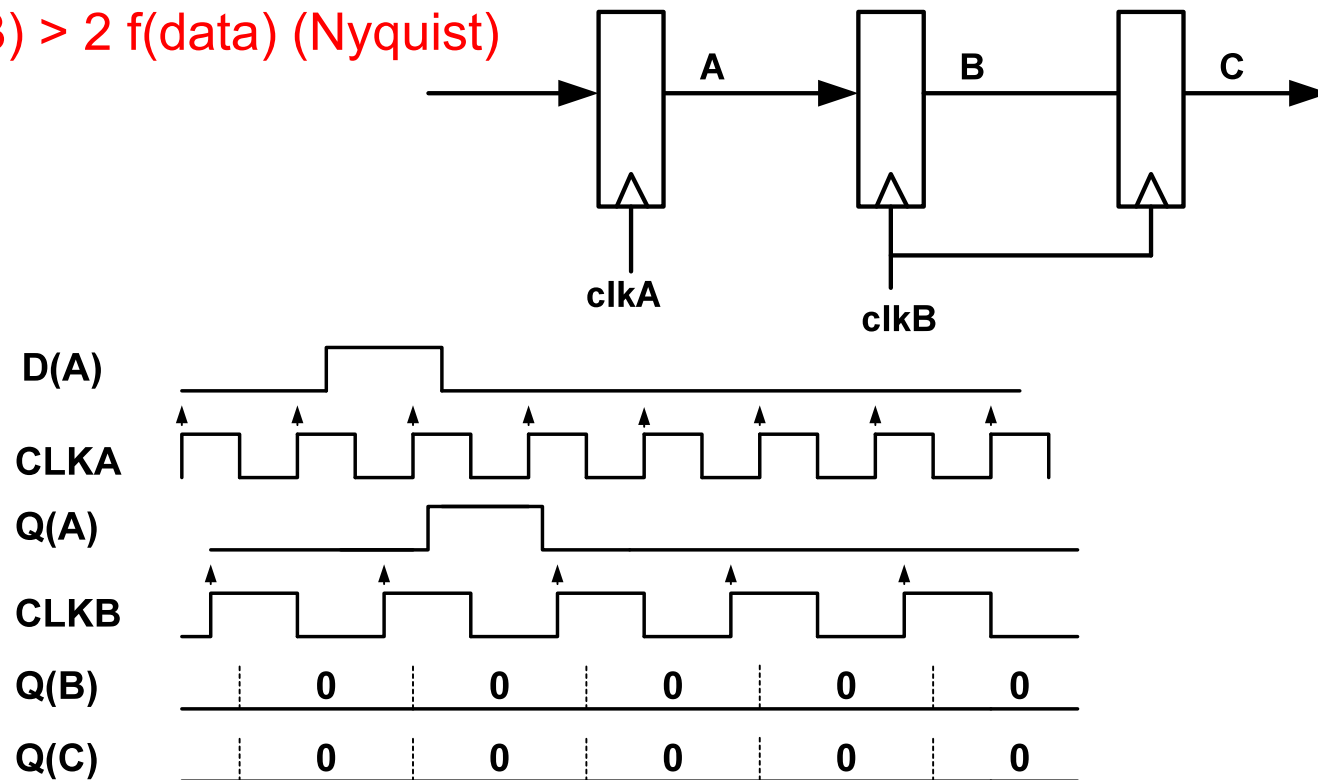
- Also slows the sample rate / transfer rate

Sampling Rate

- How fast does your sample clock need to be?

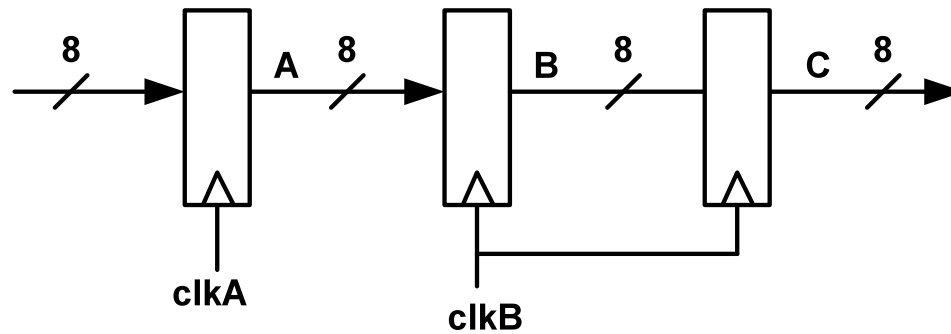# Sampling Rate

- How fast does your sample clock need to be?
    - f(clkB) > f(clkA)
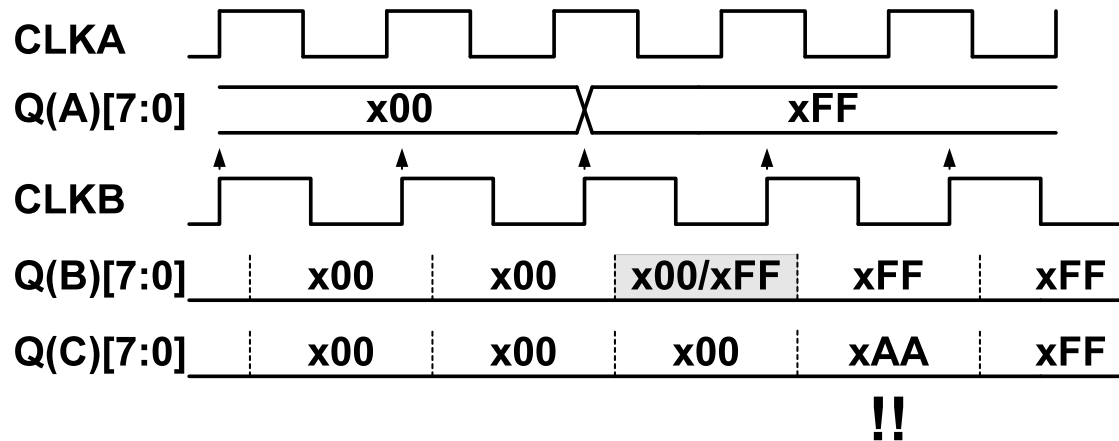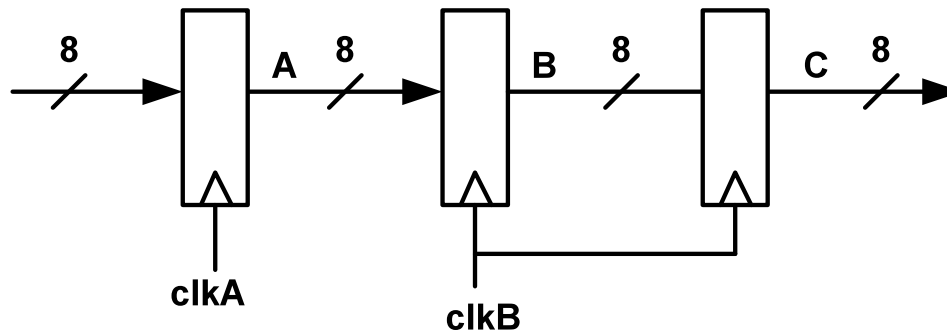   - f(clkB) > 2 f(data) (Nyquist)

More Asynchronous inputs

- Can we input asynchronous data values with several bits?

MORE ASYNCHRONOUS INPUTS

- How can we input asynchronous data values with several bits?

What Went Wrong?

- Each bit has a different delay
    - Wire lengths differ
    - Gate thresholds differ
    - Driver speeds are different
    - Register delays are different
        - Rise vs. Fall times
    - Clock skews to register bits
- Bottom line – "data skew" is inevitable
    - aka Bus Skew
    - Longer wires => More skew
- What is the solution??

Sending Multiple Data Bits

- Must send a "clock" with the data
    - Waits until data is stable
    - De-skewing delay
- **f(clkB) > 2 f(clkA)**
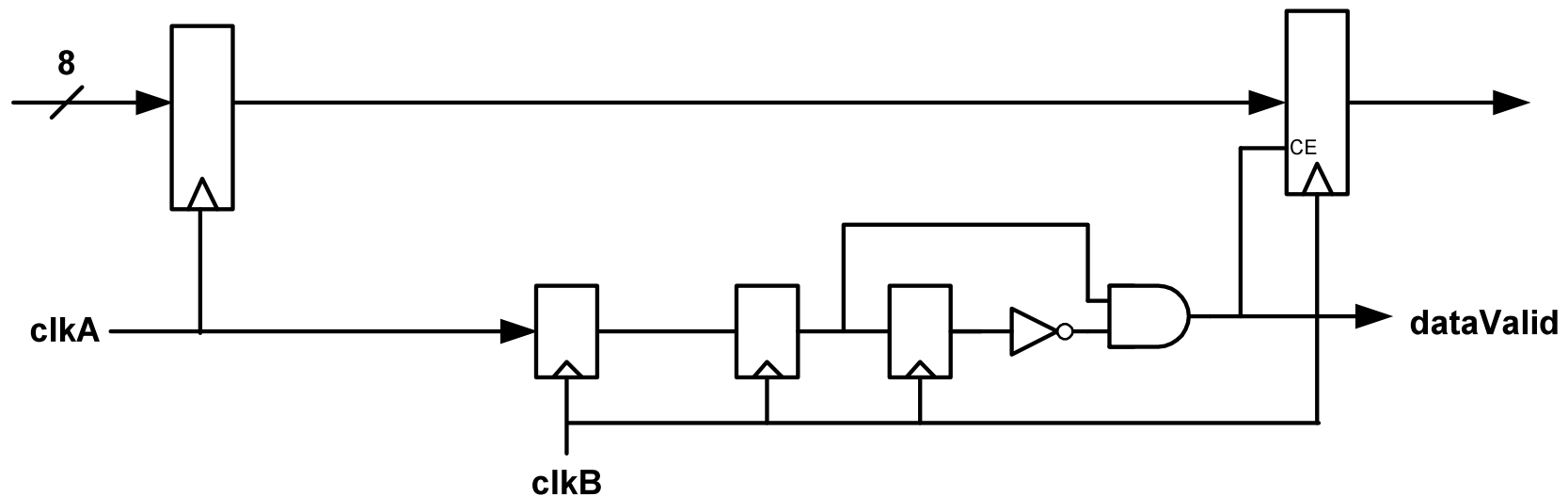
Sending Multiple Data Bits

- Balancing path delays can increase data rate
- Requires careful analysis of clock rates and delays to make sure data is stable when sampled

Sending Multiple Data Bits

- Slightly different alternative . . .