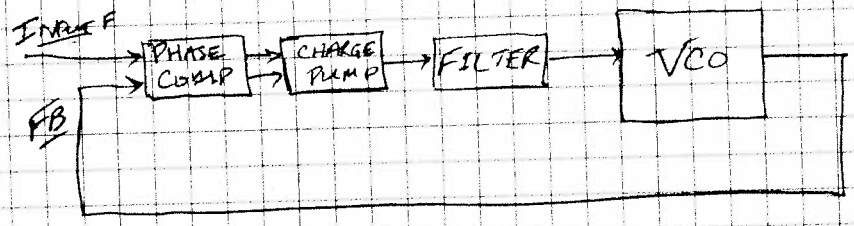
Clocking Magic with PLL's

Phase-Locked Loop

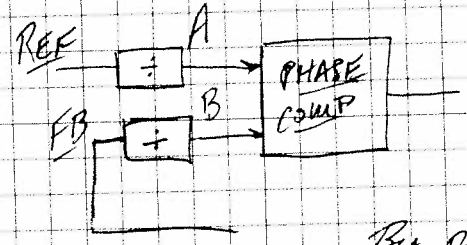


VCO - Voltage Controlled Oscillator
eg. Ring Oscillator
Higher V_{DD} → Faster operation
eg. Freq = 1.6 GHz → 3.2 GHz.

Phase Comparator: Depending on phase difference increase/decrease voltage

too fast ⇒ decrease V too slow ⇒ increase V

Use #1: Generate Multiple frequencies.



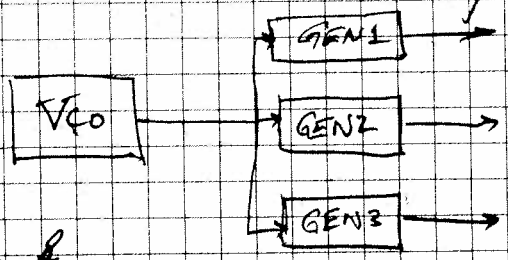
$f_{REF}/A = f_{VCO}/B$

$f_{VCO} = f_{REF} \times B/A$.

By programming A & B, we can choose f_{VCO} almost arbitrarily.

PLL

Use #2: Generate Multiple Related Frequencies



Clock Generators

Programmable Waveforms.
Programmable Phases

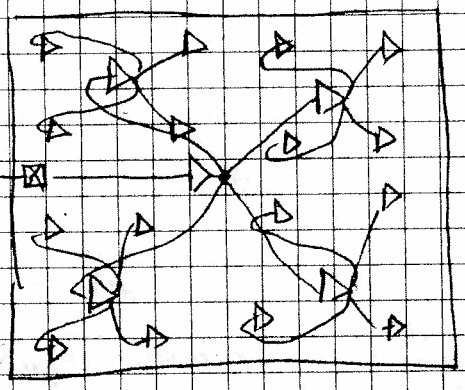
Use #3: Clock Insertion Delay Compensation.

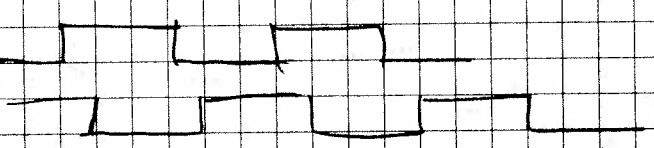
Chip clock tree: Balanced delay

Clock arrives at all registers about the same time.

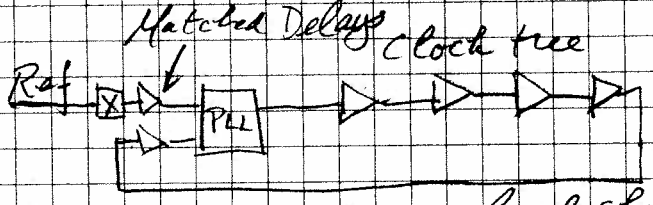
Some skew is inevitable.

However, there is a large insertion delay





Solution



PLL "copies" Reference clock to local clock.