Assignment 2

Verilog HDL for an ALU

Due: Monday, October 27, before class

The Project: Write a behavioral description for a basic 32-bit ALU. This will be the first module in your R2000 pipeline.

This definition should implement the ALU in Figure 4.21 of Hennessy and Patterson (4.18 in the first edition). That is, there should be two 32-bit operand inputs, `a` and `b`, and a 3-bit operation input. There should be a 32-bit `result` output, as well as `Zero` (all result bits 0), `Overflow` and `CarryOut` outputs. The operation coding is:

```
000  And
001  Or
010  Add
110  Subtract
111  Set (Result) on a<b
```

The difference between this solution and the previous solutions is that this should not implement any of the operations structurally, but only realize their behavior.

What should be turned in:

1. A commented version of the ALU and its tester.
2. Output from the tester that clearly indicates you have tested the ALU thoroughly.

Due: The assignment is due before class, Monday 27 October 1997. Use the Unix utility *tunin* on one of the two instructional machines orcas and sanjuan.